ESSDERC

IEEE 53rd European Solid-State Device Research Conference

September 11-14, 2023
Lisbon, Portugal

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PROGRAM

IEEE

Electron Devices Society

SEMICONDUCTORS
for an electrical and digital world

ESSDERC

IEEE 53rd European Solid-State Device Research Conference

Organized by

NOVA SCHOOL OF SCIENCE & TECHNOLOGY

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Job Listings

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Press Release

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- Our university and research programs

On behalf of the entire Organizing Committee, it is our pleasure to welcome you to the 2023 IEEE 49th European SolidState Circuits Conference (ESSCIRC) and the 53rd European SolidState Device Research Conference (ESSDERC).

NOVA School of Science and Technology of NOVA University of Lisbon and the Centre of Technology and Systems (CTS) at UNINOVA Institute, together with the University of Seville and the Institute of Microelectronics of Seville (IMSE-CNM), are the Iberian co-organizers of the IEEE ESSCIRC and ESSDERC joint Conference. This flagship European event is mainly focused on the thematic "Semiconductors for an Electric and Digital World".

Seventy-five years have passed since the invention of the transistor and twenty years have passed since its first edition in Portugal, in Estoril, in 2003, when both ESSDERC and ESSCIRC started running in parallel and had joint keynote speakers and joint focus sessions. In 2023, the conference takes place in Lisbon, at the Lisbon Congress Centre (CCL). CCL is located close to the river Tagus and the historical and cultural heritage of Belem, just a few minutes from the city center, in a prime area with a vast transport supply.

Lisbon is a historic capital, an amalgam of 800 years of cultural influences that mingle with modern trends and lifestyle creating intricate and spectacular contrasts. Spread across seven hills, always opening a window towards the majestic Tagus River. A tolerant city by tradition thanks to centuries of enjoying/experiencing cross culture influences from across the oceans. That's why Lisbon is such a great idea for hosting ESSCIRC-ESSDERC 2023. Richly captivating, Lisbon invites you to come!

The aim of ESSCIRC and ESSDERC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits, for both academia and industry researchers. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC and system designers is necessary. As a participant to ESSCIRC and ESSDERC, you not only can become familiar with the latest advances in these fields, but you will meet people who pioneered previous developments, you get access to enhance your international network in micro and nanoelectronics and you will be a witness to previews into emerging fields.

In this year of 2023, ESSCIRC-ESSDERC received a total of 380 submissions from 29 countries. From these submissions, 168 papers have been accepted (90 for ESSCIRC, 36 for ESSDERC and 42 for Joint Sessions). About 46% of the submissions came from Europe, 36% from Asia-and-Pacific, 17% from North America and 1% from Middle East, clearly demonstrating the international character of the conference. The conference has 3 Plenary Keynote Speakers coming from University of Lisbon (Técnico), Massachusetts Institute of Technology (MIT) and Monolithic Power Systems (MPS), 4 ESSCIRC Plenary Speakers coming from the University of Seville, AMD, SYNOPSYS, and University of Macao, and 3 ESSDERC Plenary Speakers coming from META Reality Labs Research, NOVA University of Lisbon and University of Texas at Dallas.

The selected papers are presented in 41 regular sessions and 1 special session (from IEEE A-SSCC). Monday, September 11, will be dedicated to the Educational Events comprising 6 Tutorials, 7 Workshops, 4 Dissemination Sessions related to EU funded projects and one full day on "Circuits Insights" IEEE SSCS initiative devoted to undergraduate students. These give extra opportunities for updating your knowledge of the state-of-the-art in the covered areas. Finally, the recent health and supply crisis have demonstrated the importance of the Semiconductor sector for the EU Societal needs and Industrial base. The idea that their supply chain is just a commodity has finally shown its limit in case of major political or economic difficulties. The EU Chips Act is a response by the EU Commission and Member States to the current situation. This hot topic will be widely addressed during our Conference, with emphasis on the actions and programs running in Portugal and Spain, two countries which may contribute a lot to reinforce Microelectronics industry in Europe.

The program also includes an outstanding social program with a Welcome Reception, at the Museum of Art, Architecture and Technology (MAAT) which is located on the riverfront of Belem historic district in Lisbon, and a Conference Banquet at the Xabregas Palace – one of the biggest icons of Portuguese history. These social events will offer ample opportunities for networking.

We thank the IEEE SolidState Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) that are the official sponsors of ESSCIRC and ESSDERC, respectively. We also thank all financial and external Sponsors who have provided the additional support allowing us to offer all the extra benefits and conditions that beyond doubt will make ESSCIRC-ESSDERC 2023 a memorable event in a long tradition for our solid-state circuits and devices community.

We would also like to thank the Steering Committee of ESSCIRC-ESSDERC for giving us the opportunity to organize this event and for many valuable recommendations and discussions.

We are very grateful to the excellent collaboration with the exceptional members of the Organizing Committee and the Technical Program Committee (TPC). All members have been extremely devoted and have worked very hard to make ESSCIRC-ESSDERC 2023 yet another successful event. Without their dedication, enthusiasm, and professionalism, this would not have been possible. We also thank all collaborators and volunteers who have helped us out.

Last but not least, we would like to express our deepest gratitude to Sistema Congressi, particularly to Sabrina De Poli and Marisa Santori, for their great professionalism, continuous dedication and commitment that allowed us to perform into continuity another ESSCIRC-ESSDERC conference as (hopefully) an exceptional and memorable event.

Finally, the real success of a conference is based on the trust of all the authors who submitted papers to the conference and on their willingness to come share their knowledge and insights. We strongly acknowledge the efforts of all our solid-state circuits and devices community to stay together and attend this new edition of ESSCIRC-ESSDERC, last of its name. Enjoy the 2023 edition of ESSCIRC-ESSDERC and your visit to Lisbon, PORTUGAL, and after enjoying and savoring this year's program, we hope to see you all again in Bruges, Belgium, for the next year edition, rebranded, ESSERC 2024.

José Epifânio da Franca
Honorary Chair – ESSCIRC-ESSDERC 2023

João Goes, José M. de la Rosa and **Andreia Cathelin**
Conference General Chairs – ESSCIRC-ESSDERC 2023

Jorge Fernandes
TPC Chair – ESSCIRC-ESSDERC 2023

João Pedro Oliveira and **Arantxa Otin**
TPC co-Chairs – ESSCIRC 2023

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TPC co-Chairs – ESSDERC 2023

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Luís B. Oliveira, Pedro Santos, Rui Santos-Tavares and **João de Melo**
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Local Arrangement Co-Chair: Rui Santos-Tavares (Univ. Nova de Lisboa, UNINOVA, PT)
Local Arrangement Co-Chair: João de Melo (CERN, CH)

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ESSDERC TECHNICAL PROGRAM COMMITTEE

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Klaus Knobloch (Infineon Technologies, Germany)
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Rosana Rodriguez (UAB, Spain)
Dimitris Tsoukalas (NTUA, Greece)
Zhenxing Wang (AMO, Germany)
Qing-Tai Zhao (Jülich, Germany)

Track 2 – Analog, Power ad RF Devices
Mikael Östling (KTH, Sweden)
Breandán Óg Ó hAnnaidh (Analog Devices, USA)
Cezar Zota (IBM, Switzerland)
Christoforos Theodorou (IMEP, France)
Erik Lind (University of Lund, Sweden)
Frederic Allibert (SOITEC, France)
Jean-Pierre Raskin (KU Leuven, Belgium)
Michael Waltl (TU Vienna, Austria)
Nadine Collaert (IMEC, Belgium)
Susanna Reggiani (University of Bologna, Italy)
Jörg Schulze (Friedrich-Alexander University, Germany)

Track 3 - Compact Modeling and Process/Device Simulation
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Mansun Chan (UST Hong Kong, China)
Wladek Grabinski (MOS-AK, Switzerland)
Benjamin Iñiguez (University Rovira i Virgili, Spain)
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Sadayuki Yoshitomi (MegaChips, Japan)
Zhiping Yu (Tsinghua University, China)

Track 11 - Emerging and In-Memory Computing Devices & Circuits

Krishna Bhuwalka (Huawei, Belgium)
Veeresh Deshpande (Helmholtz Center Berlin, Germany)
David Esseni (University of Udine, Italy)
Andreas Fuhrer (IBM, Switzerland)
Lotte Geck (Jülich, Germany)
Elena Gnani (University of Bologna, Italy)
Per-Erik Hellstrom (KTH, Sweden)
Louis Hutin (CEA, France)
Adrian Ionescu (EPFL, Switzerland)
Joachim Knoch (RWTH Aachen University, Germany)

Track 12 - Devices & Circuits for AI and ML

Jan Hoentschel (GlobalFoundries, Germany)
Ali Khakifirooz (Intel, USA)
Manuel Le Gallo (IBM, Switzerland)
Alessandro Sottocornola Spinelli (Politecnico di Milano, Italy)
Elisa Vianello (CEA, France)
Christian Zambelli (University of Ferrara, Italy)

Track 13 - Devices and Circuits for Sensors, Optoelectronics and Display

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Clara Moldovan (Sensirion, Switzerland)
Radu Sporea (University of Surrey, United Kingdom)
Sara Pellegrini (STMicroelectronics, United Kingdom)
Ali Saeidi (Swistor, Switzerland)

Lisbon is a historic capital, an amalgam of 800 years of cultural influences that mingle with modern trends and lifestyle creating intricate and spectacular contrasts. Spread across seven hills, always opening a window towards the majestic Tagus river. A tolerant city by tradition thanks to centuries of enjoying/experiencing cross culture influences from across the oceans. We make people feel at home!

If you're dreaming about your next trip to Europe, come and discover Lisbon, a historical city full of stories to tell, where the sun shines 290 days a year and the temperature rarely drops below 15ºC. A city where you feel safe wandering around day or night, where the cuisine is dedicated to creating over a thousand ways to cook the beloved bacalhau (salted cod), and where you'll find hotels and restaurants to suit every taste, budget and requirement.

Lisbon International Airport is located still within the city boundaries only 7 kms from the city centre and from most of the conference hotels and congress centres. All Lisbon hotels are situated in the city itself. Furthermore, Lisbon has the best Hostels in the World which can be a convenient and cheaper accommodation.

Due to the influence of the Atlantic Ocean, Lisbon has a pleasant climate throughout the year. In mid September the weather is typically above 20ºC with no precipitation.

That's why Lisbon is such a great idea for Hosting **ESSCIRC/ESSDERC 2023**. You get a great venue centre and hotels that satisfy the most demanding requirements, and a surprising and welcoming city, packed with interesting things to do, getting the best of both worlds: pleasure and work.

Richly captivating, *Lisbon* invites you!

PUBLIC TRANSPORTS

Metro
Everyday from 06:30 am to 01:00 am.
More info at https://www.metrolisboa.pt/en/

Trains
Everyday from 05:00 am to 01:00 am.
More info at https://www.cp.pt/passageiros/en

Buses
Everyday from 05:30 am to 12:30 am. Night service from 12:30 am to 05:30 am.
More info at https://www.carris.pt/en/

Taxi Voucher
Taxi Voucher is a pre-paid service, only available at Turismo de Lisboa *Askme Lisboa desk*, located at Lisbon's Airport Arrivals Hall, with fixed prices, settled by the protocol between Antral, Federação Portuguesa do Táxi and Turismo de Lisboa.
https://shop.visitlisboa.com/pages/taxi-voucher

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LISBON CONGRESS CENTRE

The Congress center is located close to the river Tagus and the historical and cultural heritage of Belem, just a few minutes from the city center.

Lisboa Congress Centre - CCL is the largest congress centre in Lisbon with a total area of 29.000sqm., including 8 auditoria, 5 pavilions and 34 meeting rooms.

It has been designed to host National and International conventions, congresses, seminars, exhibitions and meeting of different sizes. It offers flexibility, maximum comfort and efficiency which allows the holding of several and different events simultaneously.

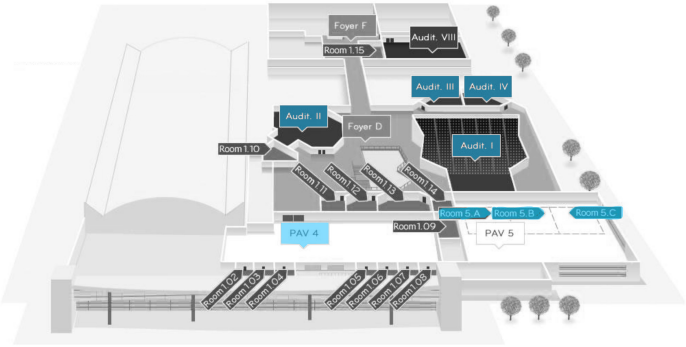
CCL, located in the historical area of **Belém, by the Tagus Rive**r, has two parking lots with 1.100 spaces and a river-view restaurant for 400. The venue is featured with the latest in technology (audiovisual and IT equipments).

Contacts:

Praça das Industrias 1, 11300-307 - Lisboa

Tel: (+351) 218 921 400

Email: lisboacc@ccl.fil.pt



PUBLIC TRANSPORTS:
Directions to Carris C 09504 - R. Junqueira (Centro Congressos) (Lisboa) with public transportation

The following transit lines have routes that pass near Carris C 09504 - R. Junqueira (Centro Congressos)

- **Bus Lines:** 201; 714; 751; 756 - Bus stop: R. Junqueira (Centro Congressos)
- **Tram Line:** 15E - Tram stop: R. Junqueira (Centro Congressos)
- **Train Line:** CASCAIS - CAIS DO SODRÉ - Train stops: Belém (20 mins walk) / Alcântara-Mar (15 mins walk)

CAR PARK:
The CCL is accessible via Portugal's main national highways, the A5, A2, and the Ponte 25 de Abril (The April 25th Bridge).

For your convenience, the CCL has an underground parking garage and an unenclosed lot, with 1,100 spaces.

The parking lots are equipped with a fire protection system and carbon monoxide detection system with extraction ventilators triggered automatically by elevated carbon monoxide levels.

- **Sessions, Tutorials, Workshops** will take place in the Conference Venue Lisbon Congress Centre (CCL).

- **Registration Desk**

  Registration Desk will be located close to the entrance of the conference venue.

- **Lunches and Coffee Breaks**

  Lunches and Coffee Breaks? will be server in the conference venue foyer (Monday to Thursday).

- **Young Professionals (YP) and Women in Engineering (WiE)**

  Tuesday, September 12th, 17:50 – 18:50, Auditorium II

  Registration Required. **Sponsored by the IEEE Solid-State Circuits Society and the Young Professionals**

- **Farewell Coffee Break**

  Thursday, September 14th, 17:10 – 17:50

- **Sabanci University (Turkey) Alumni and Friends Meeting @ ESSDERC/ESSCIRC 2023**

  Tuesday, September 12th, 17:45 – 19:00
  Room: 1.05
  Chair: Yusuf Leblebici, Sabanci University, Turkey

  As the leading privately-funded research university in Turkey in the domain of Microelectronics and Computer Engineering, Sabanci University will be hosting this informal gathering of students, young engineers and professionals. With strong undergraduate and graduate programs producing more than 350 engineers in EE/CE disciplines each year, and with many of the alumni active in leading IC design companies worldwide, the university is organizing this satellite event to bring together the young talent with the microelectronics industry and research institutions in Europe.

- **EU CHIPs ACT Panel**

  Wednesday, September 13th, 17:50 – 18:50, Auditorium I

This edition of the conference is mostly focused on the thematic "Semiconductors for an Electrical and Digital World" and it will be co-organized by NOVA School of Science and Technology of NOVA University of Lisbon and the Centre of Technology and Systems (CTS) at UNINOVA Institute, together with the University of Seville and the Institute of Microelectronics of Seville (IMSE-CNM). These Iberian co-organizers are lead institutions in their countries and the South of Europe in research and development in Microelectronics and we think that the EU Chips Act is a great opportunity to address how this funding program is running in Portugal and Spain. We firmly think that our countries must contribute a lot to reinforce the Microelectronics industry in Europe, promoting education activities to motivate young engineers to work in chip design and attract talent to the semiconductor industry.

***Moderator:* Andreia Cathelin** (STMicroelectronics, France)

Jaime Martorell (Comisionado Especial para el PERTE de Microelectrónica y Semiconductores, Spain)

Javier Calpe (Design Center Manager at Analog Devices, Valencia, Spain)

João Varela (University Professor at Instituto Superior Técnico, Researcher at LIP & CERN and CTO of PETSYS, Portugal)

Joachim Burghartz (Director of the Institut für Mikroelektronik Stuttgart, IMS-CHIPS, Germany)

	MONDAY, 11th	TUESDAY, 12th	WEDNESDAY, 13th	THURSDAY, 14th
8:30		REGISTRATION	Plenary Keynote 3	ESSCIRC Keynote 3
8:40				
8:50				
9:00		OPENING		
9:10			changing room	Awards & Next Edition
9:20		Plenary Keynote 1	MORNING SESSIONS (4 PAPERS) *(in parallel)*	
9:30				changing room
9:40	REGISTRATION			MORNING SESSIONS (3 PAPERS) (in parallel)
9:50				
10:00		Plenary Keynote 2		
10:10				
10:20				
10:30				
10:40		COFFEE BREAK	COFFEE BREAK	COFFEE BREAK
10:50	TUTORIALS, WORKSHOPS, DISSEMINATION EVENTS & CIRCUITS INSIGHTS			
11:00		MORNING SESSIONS (5 PAPERS) *(in parallel)*	MORNING SESSIONS (5 PAPERS) *(in parallel)*	MORNING SESSIONS (5 PAPERS) *(in parallel)*
11:10				
11:20				
11:30				
11:40				
11:50				
12:00				
12:10				
12:20				
12:30	LUNCH BREAK			
12:40				
12:50				
13:00		LUNCH BREAK	LUNCH BREAK	LUNCH BREAK
13:10				
13:20				
13:30	TUTORIALS, WORKSHOPS, DISSEMINATION EVENTS & CIRCUITS INSIGHTS			
13:40				
13:50				
14:00				
14:10				
14:20		ESSDERC Keynote 1	ESSCIRC Keynote 2	ESSDERC Keynote 3
14:30				
14:40				
14:50		changing room	changing room	
15:00				ESSCIRC Keynote 4
15:10				
15:20		AFTERNOON SESSIONS (4 PAPERS) *(in parallel)*	AFTERNOON SESSIONS (4 PAPERS) *(in parallel)*	
15:30	COFFEE BREAK			changing room
15:40				
15:50				AFTERNOON SESSIONS (4 PAPERS) *(in parallel)*
16:00				
16:10				
16:20				
16:30	TUTORIALS, WORKSHOPS, DISSEMINATION EVENTS & CIRCUITS INSIGHTS	COFFEE BREAK	COFFEE BREAK	
16:40				
16:50				
17:00		ESSCIRC Keynote 1	ESSDERC Keynote 2	FAREWELL COFFEE BREAK
17:10				
17:20				
17:30				
17:40		changing room	changing room	
17:50				
18:00		WiE & YP & Other Events	EU CHIPS ACT Panel	
18:10				
18:20				
18:30				
18:40				
19:30		WELCOME RECEPTION 19:30 – 21:30	GALA DINNER 19:30 – 23:00	
20:00				
20:30				
21:00				
21:30				
22:00				
22:30				
23:00				

Monday September 11, 2023 — Tutorials (T) and Workshops (W), Dissemination Events (D), and Circuit Insights

ROOM	Auditorium III	1.04	5A	5B	5C	1.05	1.06	1.07	1.08	Auditorium IV
09:30 - 10:00	Registration									
10:00 - 12:30	**T1** Radiation Hardening Techniques for Space Grade Ics	**T2** The Pavlin Cell: A Versatile Analog Building Block for Power Conversion Applications	**T3** Open-Source Neuromorphic Circuit Design Overview, Trends, and Opportunities	**W5** EUROPRACTICE Workshop Design IP Sharing and Chiplets	**T5** State-of-the-Art Methodologies for Modeling, Design, Simulation and Debug of Analog/Mixed-Signal Circuits	**T6** Power Delivery Network Optimization for 5G Applications	**W1** Technologies and Circuits for 5G Evolution to 6G	**W2** Multi-Gigabit Optical Communications for Automotive	**D1** Emulating, Listening and Communicating with Neurons	Circuit Insights
12:30 - 13:30	LUNCH BREAK									
13:30 - 15:30	**T4** Continuous-Time Pipeline ADCs: From Fundamentals to Practical Implementations	**D4** European Strenghts and Gaps in Emerging Semiconductor Technologies	**D2** Technologies, Devices, Circuits, and Algorithms for Neuromorphic Event-Based Vision System	**W3** FinFETS from Cryo-CMOS to AI	**W4** Towards Self Contained Recognition Integrated Classifiers for Smart Sensors	**W6** Source-Gated Transistors: The Building Block of Next-Generation Thin-Film Edge Processing Systems	**D3** Technologies Enabling Future Mobile Connectivity & Sensing	**W2** Multi-Gigabit Optical Communications for Automotive	**D1** Emulating, Listening and Communicating with Neurons	Circuit Insights
15:30 - 16:00	COFFEE BREAK									
16:00 - 18:00	**W7** MOS-AK Workshop	**D4** European Strenghts and Gaps in Emerging Semiconductor Technologies	**D2** Technologies, Devices, Circuits, and Algorithms for Neuromorphic Event-Based Vision System	**W3** FinFETS from Cryo-CMOS to AI	**W4** Towards Self Contained Recognition Integrated Classifiers for Smart Sensors	**W6** Source-Gated Transistors: The Building Block of Next-Generation Thin-Film Edge Processing Systems	**D3** Technologies Enabling Future Mobile Connectivity & Sensing	**W2** Multi-Gigabit Optical Communications for Automotive	**D1** Emulating, Listening and Communicating with Neurons	Circuit Insights

Tuesday, September 12, 2023

ROOM	Auditorium II	Auditorium III	Auditorium IV	5A	5B
08:30 - 09:00	REGISTRATION				
09:00 - 09:20	OPENING				
09:20 - 10:00	**A1L-0** (Auditorium I) Plenary Keynote 1: José Epifânio da Franca European Semiconductor Innovation and Entrepreneurship 20 Years Past, 20 Years Ahead				
10:00 - 10:40	**A2L-0** (Auditorium I) Plenary Keynote 2: Muriel Médard Bringing Circuits and Communications Back Together, in a Modular Fashion				
10:40 - 11:10	COFFEE BREAK				
11:10 - 12:50	**A3L-1** Sensor Interfaces	**A3L-2** Advanced Devices	**A3L-3** Analog-in-Memory Computing	**A3L-4** RF Transceivers	**A3L-5** Beyond 100GHz Communication
12:50 - 14:20	LUNCH BREAK				
14:20 - 15:00	**A4L-0** (Auditorium I) ESSDERC Keynote 1: Barbara de Salvo New Technologies and Innovative Architectures for the Augmented Reality, the Next Human-Machine Interfaces				
15:00 - 15:10	changing room				
15:10 - 16:30	**A5L-1** References	**A5L-2** Memory 1	**A5L-3** Imagers & Vision Sensors	**A5L-4** Devices & Circuits for Emerging Technologies	**A5L-5** Frequency Sources
16:30 - 17:00	COFFEE BREAK				
17:00 - 17:40	**A6L-0** (Auditorium I) ESSCIRC Keynote 1: Dino Toffolon High speed Wireline Transceivers Past, Present and Future Wireline SerDes Transceivers: Evolution and Prospects for 224-Gb/s				
17:40 - 17:50	changing room				
17:50 - 18:50	Women In Engineering & Young Professionals (Auditorium II)				

19:30 21:30	WELCOME RECEPTION MAAT – Museum of Art, Architecture and Technology

Wednesday, September 13, 2023

ROOM	Auditorium II	Auditorium III	Auditorium IV	5A	5B	5C
08:30 - 09:10	**B1L-0** **(Auditorium I)** **Plenary Keynote 3: Eric Yang** **The Heart of Artificial Intelligence Advanced Power Semiconductors Enable Greener, Denser, and Smarter Datacenters**					
09:10 - 09:20	changing room					
09:20 - 10:40	**B2L-1** **Boosting SAR A/D Converters**	**B2L-2** **Compact Modeling**	**B2L-3** **Biosensing & Photodetectors**	**B2L-4** **Cryogenic Circuits & Systems for Quantum Computing**	**B2L-5** **Wireline Techniques**	**B2L-6** **Communication & Cryptography Circuits**
10:40 - 11:10	**COFFEE BREAK**					
11:10 - 12:50	**B3L-1** **Analog Techniques**	**B3L-2** **Numerical & Statistical Modeling**	**B3L-3** **Digital & Analog AI Processors**	**B3L-4** **Power Techniques & LDO**	**B3L-5** **Frequency Synthesizers**	
12:50 - 14:20	**LUNCH BREAK**					
14:20 - 15:00	**B4L-0** **(Auditorium I)** **ESSCIRC Keynote 2: Brendan Farley** **Software Defined Radio for Next Generation Communication Networks**					
15:00 - 15:10	changing room					
15:10 - 16:30	**B5L-1** **Novel Hybrid A/D Converters**	**B5L-2** **Memory Device Modeling**	**B5L-3** **Biosensors**	**B5L-4** **Power for Medical & IoT**	**B5L-5** **RF Si Device Technology**	
16:30 - 17:00	**COFFEE BREAK**					
17:00 - 17:40	**B6L-0** **(Auditorium I)** **ESSDERC Keynote 2: Pedro Barquinha** **Oxide Thin-Film Transistors: Are we Reinventing Electronics? Or Dressing an Old Story with Today's Clothes?**					
17:40 - 17:50	changing room					
17:50 - 18:50	**EU CHIPS ACT** **Panel** **(Auditorium I)**					

19:30 23:00	**GALA DINNER** **XABREGAS PALACE**

Thursday, September 14, 2023

Room	Auditorium II	Auditorium III	Auditorium IV	5A	5B	5C
08:30 - 09:10	**C1L-0** **(Auditorium I)** **ESSCIRC Keynote 3: Ángel Rodríguez-Vázquez** **Chip Architectures for Efficient Analog-to-Information Image Analysis using Out-the-Box Processing Concepts**					
09:10 - 09:20	Awards Ceremony - Auditorium I					
09:20 - 09:30	Presentation on ESSERC 2024 - Audutorium I					
09:30 - 09:40	changing room					
09:40 - 10:40	**C2L-1** Innovations in High-Speed A/D Converters	**C2L-2** Application Specific SoCs	**C2L-3** Biomedical & Wearable Sensors	**C2L-4** VCSEL Transmitters	**C2L-5** Advanced CMOS LNA Techniques	**C2L-6** Memory 2
10:40 - 11:10	COFFEE BREAK					
11:10 - 12:50	**C3L-1** Advances in Delta-Sigma Converters	**C3L-2** A-SSCC Special Session	**C3L-3** SRAM Digital Computing in Memory	**C3L-4** DC-DC Converters	**BC3L-5** mm-Wave Phased Array Techniques	
12:50 - 14:20	LUNCH BREAK					
14:20 - 15:00	**C4L-0** **(Auditorium I)** **ESSDERC Keynote 3: Kenneth O** **Silicon Technology Innovation Opportunities for Applications at 0.1 to 1 THz Beyond that for Transistors**					
15:00 - 15:40	**C5L-0** **(Auditorium I)** **ESSCIRC Keynote 4: Rui P. Martins** **Analog and Mixed-Signal CMOS Circuits:** **The Emergence and Leadership of a Lab, a Reference Book and the Future at the Core of the A/D Interface in the IoE**					
15:40 - 15:50	changing room					
15:50 -17:10	**C6L-1** Optoelectronic Device Modeling	**C6L-2** Memory Design & In-Memory Computing	**C6L-3** ADC & RF Interface	**C6L-4** mm-Wave Transceivers	**C6L-5** Power & RF Devices: From Substrate to Packaging	
17:10 - 17:50	FAREWELL COFFEE BREAK					

CERTIFICATE OF ATTENDANCE
Certificates must be requested to essxxrc@sistemacongressi.com after the Conference.

LANGUAGE
The official language of the conference is English: no simultaneous translation will be available.

REGISTRATION DESK
The Registration Desk is located at the main entrance of the Conference Venue, Lisboa Congress Centre - CCL Due to the large number of registered participants, we invite all attendees to arrive well in advance to avoid queues and delays. The registration desk will be open from Monday -Wednesday from 8:30 to 17:00. Thursday from 8:00 to 15:00.

BADGES
Badges must always be visibly worn during sessions, coffee breaks and lunches at the conference site but also during social program activities.

COFFEE BREAKS AND LUNCHES
Coffee breaks and lunches will be served to registered participants wearing their badges. Accompanying persons have no access to scientific sessions nor to coffee breaks and lunches.

Please note that vegetarian dishes will be on daily menu; for other special needs, we will try to serve a good variety of food so that it will be easier for you to get some alternatives in case of special diet restrictions.

PERSONS WITH SPECIAL NEEDS
Every effort has been made to ensure that people with special needs are catered for during the conference. Should you require any specific assistance, please let us know in advance to enable to assist in making your stay at the conference a pleasant and comfortable one.

INTERNET / WI-FI
Wi-Fi connection will be available on site.

CURRENCY
The local currency is € (Euro). Automatic teller machines and exchange offices are available all over the city. Most hotels, restaurants and shops accept major credit cards but please always check first!

ELECTRICITY
230 / 400 volts, on a 50-hertz frequency. The electric sockets adhere to European standards. Blade plugs (US standard) must be used in conjunction with a 230 volts transformer, as well as an adaptor.

WEATHER
In Lisboa winters are mild and summers hot, though moderated by its location near the sea. During spring and autumn there are usually sunny days with mild temperatures.

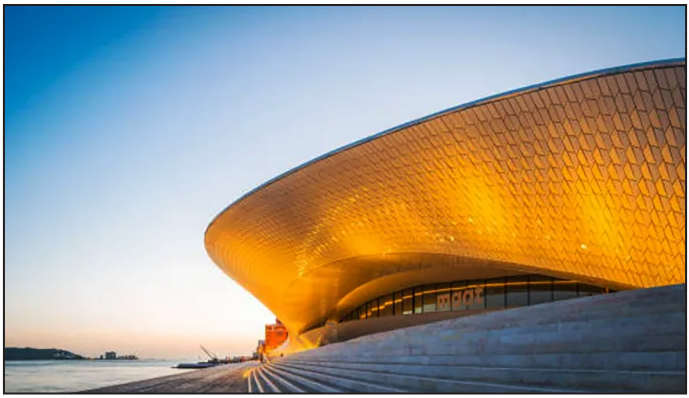
CALLING CODES
International Calls: 00 + country area code
Portugal area code: +351

EMERGENCY NUMBERS
National Emergency Number: 112
Public Health Line 24: (+351) 808 24 24 24

LIABILITY
In registering for the conference, participants agree that neither the Organizing Committees nor the Organizing Secretariat assumes any liability.

WELCOME COCKTAIL - Tuesday 12 September 2023

MAAT – Museum of Art, Architecture and Technology



The Museum of Art, Architecture and Technology (MAAT) is located on the river-front of Belém historic district in Lisbon, flanked by Av. Brasília and the railway that connects Cais do Sodré to Cascais. The best way to get to MAAT is by public transport, bus, train or tram, which always involves a short walk over one of the two pedestrian bridges available in the area. The fastest route is through the passage that connects Rua da Junqueira, where the bus and tram stop Altinho (MAAT) is, directly to the roof of MAAT. This footbridge was designed by the architects AL_A (Amanda Levete Architects), the authors of the museum's new building. Alternatives such as bicycle, scooter, or car, may also be options. Parking in the area is limited.

Time
19:30 - 21:30

Address
Av. Brasília, 1300-598 Lisboa
Only 10 mins walking distance from the venue!

Public Transport
Bus:
201, 714, 727, 751 – Altinho stop (MAAT)
728 – Belém River Station Stop

Tram:
15E, 18E – Altinho Stop (MAAT)

Train:
Belém Station (Cascais Line)

Boat:
Belém River Station (Belém – Porto Brandão – Trafaria)
Line 1, 2, 4, 12, 14, 27

Rate
- included in the conference registration fee.
- Additional ticket for accompanying person: € 75.

GALA DINNER - Wednesday 13 September 2023

PALÁCIO DE XABREGAS

Located to the east of Lisbon's Center, the Xabregas Palace is one of the biggest icons of Portuguese history.

Between the 15th and 19th centuries, Xabregas was an area known for recreational farms and large convents of Lisbon, which, due to its location next to the Tagus River, allowed a quick and comfortable journey to the city center as well as to the south and inside areas of the country.

In the 17th century, when it was owned by the Melo, the Monteiro-Mor of the Kingdom, this palace was the scene of several meetings of the conspirators who restored the Independence of Portugal in 1640.

In this imposing architectural ensemble of Mannerist taste, which largely withstood the earthquake of 1755, decorative arts stand out, such as tiles from the second half of the 17th century and the first half of the 18th century, and mural painting from the first and second half of the 19th century that make this palace a unique example of its kind.

Time
19:30 - 23:00

Address
Rua de Xabregas 40, 1900-438 Lisboa

Public Transport
Bus:
794, 718, 781, 759 – Xabregas Stop
Lines Maps at carris.pt

Rate
- included in the conference registration fee.
- Additional ticket for accompanying person: € 150.

SEMICONDUCTORS
for an electrical and digital world

The aim of **ESSCIRC** and **ESSDERC** is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary.

ESSCIRC and **ESSDERC** are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both device and circuit communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

The conference has 3 Plenary Keynote Speakers coming from University of Lisbon (Técnico), Massachusetts Institute of Technology (MIT) and Monolithic Power Systems (MPS), 4 ESSCIRC Plenary Speakers coming from the University of Seville, AMD, SYNOPSYS, and University of Macao, and 3 ESSDERC Plenary Speakers coming from META Reality Labs Research, NOVA University of Lisbon and University of Texas at Dallas.

ESSCIRC-**ESSDERC** evolves, following recent R&D device/circuit fast-growing topics, and creating even more interactions between circuit and device as well as memory and logic researchers.

Technical Program Committee tracks have been re-organized accordingly and joint tracks between **ESSCIRC** and **ESSDERC** will be proposed.

ESSCIRC-**ESSDERC** encourages submissions in all areas with special emphasis on:

- **Joint tracks Circuits and Devices: Neuromorphic Computing, advanced memories, AI Accelerators, in-Memory-Computing, Security Advanced Computing Devices and Circuits: Advanced CMOS, post-CMOS, Quantum Computing Sensors, MEMS, Bio-electronics, Biomedical Optoelectronics, Display and Imaging**
- **Analog circuits, Data converters, RF and mm-wave circuits, Frequency generation, Wireless and wireline systems, Power management**
- **Analog, Power and RF devices, Electron Device Simulation and Modeling, Advanced Technology, Process and materials**

Student papers are welcome: a special student session will be organized by **ESSCIRC** and **ESSDERC** in 2023. The venue of the conference events, including workshops and tutorials, is Lisbon Congress Center (CCL). The Congress Center is located close to the river Tagus and the historical and cultural heritage of Belem, just a few minutes from the city center, in a prime area with a vast transport supply.

The working language of the conference is English.

José Epifânio da Franca
IST, Universidade de Lisboa, PT

European Semiconductor Innovation and Entrepreneurship 20 Years Past, 20 Years Ahead

Date: Tuesday 12
Time: 09:20 – 10:00
Room: Auditorium I
Chair: Jorge Fernandes *(IST, Universidade de Lisboa, PT)*

Europe has a long history of excellence in Semiconductor Innovation and Entrepreneurship. Over the past two decades, more than $11 billion have been invested in about 1,000 startups of which Dialog Semiconductor, ARM Holdings, Imagination Technologies, Silex Microsystems, Xmos, GreenWaves Technologies, Nanusens, Intellitronika are just a few among many others which have developed innovative technologies and solutions that are used in a wide range of industries and have achieved scale-up status and global prominance.

Today, possibly more than ever before, Europe can be at the forefront of disruption and innovation driven by mutually-feeding trends in AI and analog computation, IoT and edge computing, quantum and neuromorphic computing, optical processing, and solid-state photonic chips. Going forward, we will highlight the formidable challenges ahead, notably limited access to venture capital funding and value chain fragmentation, and discuss the 5 critical elements of the Entrepreneurship ecosystem that will strengthen competitiveness, drive growth and progress: Innovation, Job Creation, Competition, Flexibility, and Access to Talent.

José Epifânio da Franca

- José Franca graduated in Electrical Engineering from Instituto Superior Técnico (1978), received the Ph.D. from Imperial College London (1985), and completed the executive program on Management of Research and Technology-based Innovation at the Sloan School of Management, Massachusetts Institute of Technology (1992). He is Professor at Instituto Superior Técnico where he founded the Integrated Circuits and Systems Group (1986), and was a member of the Management Board (1987-1991). His current areas of interest and expertise include entrepreneurship and innovation.
- In 1997 José Franca co-founded and became CEO and Chairman of Chipidea Microelectronics which pioneered and became a worldwide leader in the Semiconductor Analog Mixed-Signal IP industry until his departure in 2008 upon the acquisition by MIPS Technologies. Currently with c. 700 engineers in Portugal, the former Chipidea operation is now the largest European engineering centre of Synopsys.
- In 2012 José Franca was appointed by the Government of Portugal Chairman of the Board and CEO of Portugal Ventures, which he served until 2015 with the mandate to establish a modern, internationally recognized technology-based entrepreneurial ecosystem in Portugal laying out solid foundations for the attraction of international venture capital and steady worldwide inflows of talent and experience.
- José Franca is Fellow of the IEEE (1997), recipient of the Golden Jubilee Medal (1999) and of the Industrial Pioneer Award (2010) of its Circuit and Systems Society. He is the winner of the 2008 University of Coimbra Prize, was bestowed the "Grande Oficial da Ordem do Mérito" by the President of Republic (2006), and awarded the "Doctor Honoris Causa" degree from University of Macau (2006).

Muriel Médard

MIT, US

Bringing Circuits and Communications Back Together, in a Modular Fashion

Date: Tuesday 12
Time: 10:00 – 10:40
Room: Auditorium I
Chair: Andreia Cathelin *(STMicrolectronics, FR)*

In this talk, we present a vision of standards to help ensure both reliability and room for innovation. Current development of algorithms for communications and networking are often done separately from their circuit instantiations. The circuit design in turn takes multiple algorithms and embeds them in a monolithic architecture. We argue that standards can successfully concentrate on purely functional matters, relying on modular APIs, rather than being prescriptive about methods, which often embed inefficient legacy technologies. Within these modules, we argue that there are real benefits to creating or recreating tighter links between algorithmic development and circuit design. As a case study, we present recent developments in universal error-correcting decoding using guessing random additive noise decoding (GRAND). In that project, a close collaboration between the creation of decoders and of circuits leads to schemes that outperform the state of the art.

Muriel Médard

- Muriel Médard is the NEC Professor of Software Science and Engineering in the Electrical Engineering and Computer Science (EECS) Department at MIT, where she leads the Network Coding and Reliable Communications Group in the Research Laboratory for Electronics at MIT and Chief Scientist for Steinwurf, which she has co-founded. She obtained three Bachelors degrees, as well as her M.S. and Sc.D, all from MIT. Muriel is a Member of the US National Academy of Engineering (elected 2020), a Member of the German National Academy of Sciences Leopoldina (elected 2022), a Fellow of the US National Academy of Inventors (elected 2018), American Academy of Arts and Sciences (elected 2021), and a Fellow of the Institute of Electrical and Electronics Engineers (elected 2008). She holds Honorary Doctorates from the Technical University of Munich (2020) and from The University of Aalborg (2022).
- Muriel was awarded the 2022 IEEE Kobayashi Computers and Communications Award. She received the 2019 Best Paper award for IEEE Transactions on Network Science and Engineering, the 2018 ACM SIGCOMM Test of Time Paper Award, as well as nine conference paper awards.
- Muriel currently serves as the Editor-in-Chief of the IEEE Transactions on Information Theory. Muriel was elected president of the IEEE Information Theory Society in 2012, and serves on its board of governors, having previously served for eleven years.
- Muriel received the inaugural MIT Postdoctoral Association Mentoring Award in 2022, the inaugural MIT EECS Graduate Student Association Mentor Award, voted by the students in 2013. She set up the Women in the Information Theory Society (WithITS) and Information Theory Society Mentoring Program, for which she was recognized with the 2017 Aaron Wyner Distinguished Service Award. She serves on the Nokia Bell Labs Technical Advisory Board.
- Muriel has over sixty US and international patents awarded, the vast majority of which have been licensed or acquired. For technology transfer, she has co-founded CodeOn, for which she consults, and Steinwurf, for which she is Chief Scientist.

Eric Yang

MPS, US

The Heart of Artificial Intelligence Advanced Power Semiconductors Enable Greener, Denser, and Smarter Datacenters

Date: Wednesday 13
Time: 08:30 – 09:10
Room: Auditorium I
Chair: Luís B. Oliveira *(Universidade Nova de Lisboa, PT)*

As the demand for cloud computing, AI applications, machine learning, high performance computing, and supercomputers rapidly grows, datacenters are evolving to accommodate new, higher power requirements. Meanwhile, to optimize the Total Cost of Operation (TCO), datacenters demand for higher efficiency and higher density power solutions. Power has become one of the biggest challenges for a datacenter. With the advanced power semiconductor technologies, which includes device processes, packaging technologies, and system level design optimizations, analog/digital mixed signal circuit designs including power specific state machines, sensors, high precision ADC, and DSP ASIC.

The worldwide power community has been continuously pushing the boundaries to achieve the common goal: to enable a Greener, Denser, Smarter datacenter. Think of AI processor as a brain, power engine is simply the heart.

Eric Yang

- Dr. Eric Yang received the B.S. and M.S. degree from Tsinghua University, in 1982 and 1984 respectively. In 1994, he received his PhD degree in electrical engineering from Virginia Polytechnic Institute and State University.
- He then joined Harris Semiconductor as staff applications engineer working on high power semiconductor device and module development. He moved to Silicon Valley in 1998 and joined Semtech Corp. as Senior Staff Engineer later Director of Applications, working on develop first generation of multi-phase CPU core voltage regulators.
- He joined Monolithic Power System (MPS) in 2006 as Senior Director of applications engineering and later became Vice President of Technical Marketing. In past 17 years, Dr. Yang played an essential role to build MPS engineering teams, define new products, and develop of power management system IP's. which cover computing/datacenter platforms, networking/communications, AC to DC power conversions, battery systems, automotive platforms, motor drives, and so on.

Barbara De Salvo
META, US

New Technologies and Innovative Architectures for the Augmented Reality, the Next Human-Machine Interfaces

Date: Tuesday 12
Time: 14:20 – 15:00
Room: Auditorium I
Chair: Maria Merlyne De Souza *(University of Sheffield, UK)*

The human relationship with computers and information has evolved in a dramatic way in the last decades. Humanity encountered the first personal computer in the 50s, which eventually evolved on the Internet. Recent times have seen the revolution of the smart phone. Today, we're immersed into a vast ocean of virtual information and connections whenever and wherever we want, through two-dimensional surfaces which accompany us everywhere we go. Clearly, the future of our digital gateways will be even more portable and personal in the future. At Facebook Reality Labs, we are developing the next generation computing platform, the AR/VR glasses which will combine virtual and real worlds, to serve human needs and to explore the limits of human experience. Silicon is only one piece of the many technologies that need to converge together to create a fully AR experience. We need to integrate Si together with displays, sensors, electrical and mechanical systems and not ultimately, AR algorithms. If the importance of performance-per watt is well known for mobile device, it will be even more critical for AR devices. In order to make this vision reality, we will need optimization at every level of the system, including novel revolutionary technologies and co-optimization of HW and SW.

Barbara De Salvo

- Barbara De Salvo is Director of Research at Meta Reality Labs Research (USA), responsible for Silicon Strategy and Foundry Engineering. She influences topnotch semiconductor companies and academia to define the most optimized semiconductor technologies that will enable Meta's next generation of human-machine-interface, the new Augmented Reality/Virtual Reality (AR/VR) platforms which combine virtual and real worlds to explore the limits of human experience. She leads a multi-disciplinary team, including technologists, Asic designers, Machine Learning (ML) algorithm-, Computer Vision- scientists, and system engineers to drive the introduction of novel semiconductor technologies and new computing paradigms (as Compute-In-Memory, On-Sensor-Compute) in next generation AR/VR product systems.
- Before joining Meta in 2019, she was Chief Scientist and Deputy Director of CEA-LETI (France), driving the path-finding strategy. In CEA-LETI, she founded and led the advanced memory technology division (2008-2013), where she promoted the introduction of disruptive memory technologies, such as phase-change memories, resistive oxide-based and conductive-bridge memories and neuromorphic hardware solutions based on emerging technologies.
- In 2013-2015, she was manager and visiting scholar in IBM-Albany-NY (USA) in the frame of the sub-10nm CMOS International Technology Alliance, where several of her research works have led to product technologies for novel logic ICs (as Silicon-On-Insulator, Finfet and stacked nanowire technology platforms).

- She has authored more than 350 referred articles, ten book chapters, a monography on Silicon Non-Volatile Memories edited by Wiley and Sons. She served as General Chair of IEEE IEDM 2022, as well as chair of the IEEE Corporation Award Committee (2021, 2022).
- She is a Fellow of the IEEE, and an active member of the IEEE Women in Engineering network.

Pedro Barquinha
Universidade Nova de Lisboa, PT

Oxide Thin-Film Transistors: Are We Reinventing Electronics? Or Dressing an Old Story with Today's Clothes?

Date: Wednesday 13
Time: 17:00 – 17:40
Room: Auditorium I
Chair: Radu Sporea *(University of Surrey, GB)*

With the current constrains on assuring supply of microelectronic chips and on technological/ physical limitations to further miniaturize existing Si-based transistors, the world is looking for alternative approaches to revolutionize electronics. Thin-film transistors (TFTs) have been fueling flat panel display industry for the last 3 decades, and with oxide semiconductors enabling a combination of good electrical performance, low-temperature/large area fabrication and even optical transparency, academics and industry are pushing the boundaries for these devices and taking them to applications beyond displays. Indeed, oxide TFTs are now finding their application space in multiple domains: from low-transistor count flexible circuits that can be seamlessly embedded into everyday objects, to high-density circuits with sub-10 nm gate lengths, where arguments such as compatibility with non-planar device structures (e.g., gate-all-around) and extremely low off-currents turn the technology very appealing for a new wave of electronic applications, where sustainability and high-performance can mutually exist.

Pedro Barquinha

- Pedro Barquinha received his PhD in Nanotechnologies and Nanosciences from NOVA University Lisbon in 2010. He is currently Associate Professor at the Materials Science Department of FCT-NOVA and group leader of Materials for Electronics, Optoelectronics and Nanotechnology at CENIMAT|I3N.
- Low-temperature oxide electronics has been his core research since 2004, including thin film deposition, nanostructure synthesis and their integration in flexible devices such as transistors, circuits and nanogenerators.
- This has been achieved through >40 research projects with academia and industry, including an ERC Starting Grant (TREND) and an ERC Proof of Concept Grant (FLETRAD). He co-authored more than 170 peer-reviewed papers (h-index=54, as March 2023), 3 books and 7 book chapters and is an editor at IEEE Electron Device Letters and IEEE Journal of Flexible Electronics.
- Since 2022 he is a member of the Portuguese Council for Science, Technology and Innovation and a member of the International Iberian Nanotechnology Laboratory (INL) council.

Kenneth O

Texas Instruments, US

Silicon Technology Innovation Opportunities for Applications at 0.1 to 1 THz Beyond that for Transistors

Date: Thursday 14
Time: 14:20 – 15:00
Room: Auditorium I
Chair: Arantxa Otin *(University of Zaragoza, ES)*

The wide frequency bands that can become available and smaller wavelengths at 0.1 to 1 THz hold the promise for enabling tera-bps communication, and higher resolution radar imaging in visually impaired conditions at a given form factor. This frequency range can also be utilized to detect a wide variety of gases and to measure concentrations. This presentation reviews the state of art for electronics performance in this frequency range that has rapidly advanced over the past decade. Two application examples, 420-GHz imaging and 300-GHz high bandwidth wireless communication are then examined. From this, opportunities for improvement, such as that for noise performance, output power and power efficiency, as well as additional required capabilities such as low-cost testing, packaging and electronically steerable reflectarray are identified, and the technology innovation beyond that for transistors, which can mitigate or overcome the limitations and support the additional necessary capabilities are discussed.

Kenneth O

- Kenneth O received his Ph.D. degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1989.
- From 1989 to 1994, Dr. O worked at Analog Devices Inc. developing sub-micron CMOS processes for mixed signal applications, and high speed bipolar and BiCMOS processes. He was a professor at the University of Florida, Gainesville from 1994 to 2009.
- He is currently the Director of Texas Analog Center of Excellence and Texas Instruments Distinguished University Chair Professor of Analog Circuits and Systems at the University of Texas at Dallas. His research group is developing circuits and components required to implement analog and digital systems operating at frequencies up to 40THz using silicon IC technologies.
- Dr. O was the President of the IEEE Solid-State Circuits Society in 2020 and 2021.
- He has authored and co-authored 290 journal and conference publications, as well as holding 15 patents.
- Dr. O has received the 2014 Semiconductor Research Association University Researcher Award.
- Prof. O is also an IEEE Fellow.

T1
Radiation Hardening Techniques for Space Grade ICs

Cristiano Calligaro *(RedCat Devices, IT)*

Event: Tutorial
When: 10:00 - 12:30
Where: Auditorium III

Abstract
In this tutorial an overview on radiation effects on semiconductor components will be provided under the perspective of CMOS design to mitigate hard errors like latch-up or gate rupture and soft errors (bit upsets and transients). The main radiation hardening techniques, both at circuit and layout levels, will be described with a focus on standard cells, memories (SRAMs and NVMs) and analog components (ADCs and DACs). Testing techniques under irradiation to verify effective hardness suitable for space applications will be described for TID (Total Ionizing Dose with Cobalt 60) and SEE (Single Event Effects with Heavy Ions).

Organiser
Cristiano Calligaro received the laurea degree in Electronics Engineering and the Ph.D. degree in Electronics and Information Technology Engineering from the University of Pavia (Italy) in 1992 and 1997 respectively. After obtaining the Ph.D. degree he moved to MAPP Technology. In 2006 he established RedCat Devices srl as a start-up. During his career he has been involved in memory design (volatile and non volatile) both for consumer application (multilevel flash memories) and space applications (rad-hard memories) and software design for SEE/TID evaluation using open source EDA tools. His current research interest is focused on rad-hard standard cell libraries to be used for rad-hard mixed signal ASICs, stand-alone memories (SRAMs and NVMs) and testing methodologies for rad-hard components. He holds more than 20 patents mainly in the field of multilevel NVMs and is co-author of more than 60 papers and one book (Rad-hard Semiconductor Memories, River Publishers). He has been coordinator of RAMSES and ATENA projects inside the Italy-Israel Cooperation Programme, SkyFlash project in the European FP7 Programme, EuroSRAM4Space project in the Eureka Eurostars Programme and RADPROM project funded by Italian Space Agency (ASI). In 2019 he co-founded BlackCat Beyond as a start-up company focusing on silicon dosimeters for medical and space applications. He is IEEE Senior Member and Eureka Euripides reviewer.

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T2
The Pavlin Cell: A Versatile Analog Building Block for Power Conversion Applications

Claudio Adragna *(STMicroelectronics, IT)*

Event: Tutorial
When: 10:00 - 12:30
Where: 1.04

Abstract
The Pavlin cell is a simple yet powerful analog building block, whose fundamental function is to provide a dc voltage proportional to the ratio of the duration of two time intervals. This is an extremely useful feature that is utilized in several control ICs dedicated to power conversion applications such as PWM controllers and PFC controllers. The tutorial, after describing the structure, the steady-state operation and dynamic properties of the Pavlin cell, will illustrate a number of examples of its usage in commercially available PWM and PFC controllers that demonstrate its versatility and usefulness. Both analog IC designers and IC architects may find food for thoughts.

Organiser
Claudio Adragna is a Company Fellow, Member of the Technical Staff and of the Fellow Scientific Committee of STMicroelectronics. After heading for more than 15 years the Power Conversion Applications Laboratory, he presently serves as Power Conversion Innovation Sr. Director and Technical Advisor still in the "Industrial & Power Conversion" Division.

His expertise is in ac-dc and dc-dc power conversion in consumer, computer, home appliances, lighting, and industrial segments. He is primarily concerned with the architecture definition of control ICs: PWM, quasi-resonant, resonant, and soft-switching primary controllers, PFC controllers, high-voltage switchers, synchronous rectifier drivers.

In his thirty-year career he has defined or supervised the definition of nearly a hundred products, contributing to their market introduction too. Some of these products have brought innovation and originated new trends in systems and control ICs for power conversion. This innovation effort has resulted in over two hundred international patents granted to his name.

Claudio has also authored or co-authored over eighty publications including conference papers, technical articles in journals and trade magazines, and application notes posted on STMicroelectronics' website. According to Google Scholar, they have been cited over 2500 times.

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T3

Open-Source Neuromorphic Circuit Design Overview, Trends, and Opportunities

Charlotte Frenkel *(Delft University of Technology, NL)*

Event: Tutorial
When: 10:00 - 12:30
Where: 5A

Abstract
As a bio-inspired alternative to conventional machine-learning accelerators, neuromorphic circuits outline promising energy savings for extreme-edge scenarios. While still being considered as an emerging approach, neuromorphic chip design is now being included in worldwide research roadmaps: the community is growing fast and is currently catalyzed by the development of open-source design tools and platforms. In this tutorial, we will survey the diversity of the open-source neuromorphic chip design landscape, from digital and mixed-signal small-scale proofs-of-concept to large-scale platforms. We will also provide a hands-on overview of the associated design challenges and guidelines, from which we will extract upcoming trends and promising use cases.

Organiser
Charlotte Frenkel is an Assistant Professor at Delft University of Technology, The Netherlands. She received her Ph.D. from UC Louvain, Belgium, in 2020 and was a post-doctoral researcher at UZH and ETH Zürich, Switzerland. Her research aims at bridging the bottom-up (neuroscience-driven) and top-down (engineering-driven) neuromorphic design approaches, with a focus on digital spiking neural network processor design, embedded machine learning, and brain-inspired on-device learning. She received a best paper award at ISCAS 2020, and her Ph.D. thesis was awarded the FNRS / Nokia Bell Scientific Award 2021 and the FNRS / IBM Innovation Award 2021. She is the chair of the tinyML initiative on neuromorphic engineering, is a TPC member of ESSCIRC and DATE, and serves as an associate editor for the IEEE Trans. on Biomedical Circuits and Systems.

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T4
Continuous-Time Pipeline ADCs
From Fundamentals to Practical Implementations

Shanthi Pavan *(Indian Institute of Technology Madras, IN)*

Event: Tutorial
When: 13:30-15:30
Where: Auditorium III

Abstract
First, there were discrete-time filters and delta-sigma ADCs, and then came continuous-time filters and delta-sigma ADCs. In spite of all the initial pessimism, CTDSMs are in large-scale use. The art of the discrete-time pipeline ADC, which has been the workhorse of high-speed conversion, has been perfected over the last 35 years. In spite of all the progress, fundamental problems remain – the difficulty in driving them, high-gain amplifiers, and the necessity for an anti-alias filter. The continuous-time pipeline is an ADC architecture that combines anti-alias filtering and data-conversion. It is easy to drive, and achieves this in a way that can be proven to be more power- and area- efficient than an anti-alias filter followed by a discrete-time pipeline ADC. This tutorial describes this intriguing converter architecture, compares it with competing techniques, and its prospects and challenges.

Organiser
Shanthi Pavan is the NT Alexander Chair Professor of Electrical Engineering at the Indian Institute of Technology, Madras. He is the co-author "Understanding Delta-Sigma Modulators (second edition)" which received the Outstanding Professional Book Award from IEEE Press in 2020. Shanthi has received numerous awards for his work, including the Outstanding Forum Presenter at ISSCC 2021. He serves on the Technical Program Committee (TPC) of ISSCC and on the editorial boards of the IEEE Journal of Solid-State Circuits and Solid-State Circuits Letters. He is a fellow of the IEEE.

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T5

State-of-the-Art Methodologies for Modeling, Design, Simulation and Debug of Analog/Mixed-Signal Circuits

Pietro Caragiulo *(Meta, IT)*

Event: Tutorial
When: 10:00 - 12:30
Where: 5C

Abstract
The demand for low-power SoCs in mobile consumer electronics is a main driver for CMOS scaling. For digital designs, the adoption of advanced CMOS process technologies offers clear power, performance, area, and cost (PPAC) benefits. However, porting analog/mixed-signal circuits to the latest process node only provides marginal PPAC benefits, and it comes at the expense of increased complexity and development time. Feature scaling translates to larger wire RC product, exacerbated layout-dependent effects, and reliability challenges. The analog/mixed-signal design space has gradually shifted from device-centric to interconnect-centric. In this workshop we will present the latest methodologies for modeling, design, simulation and debug of analog/mixed circuits. These methodologies lead to improved process portability, design and verification.

Organiser
Pietro Caragiulo pursued his Ph.D. degree in Electrical Engineering at Stanford University and Master and Bachelor degree at Politecnico di Bari. From 2010 to 2018, he was with the SLAC National Accelerator Laboratory, where he was involved in the development of high-frame-rate cameras and time-of-flight sensors. Dr. Caragiulo is the recipient of several awards, including the Stanford Graduate Fellowships (SGF) in Science and Engineering in 2018 and the ADI Outstanding Student Designer Award in 2020. He is currently a Silicon Research Scientist at Meta.

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T6
Power Delivery Network Optimization for 5G Applications

Jose Luis Silva, Marlon Eguia *(Monolithic Power Systems, US)*

Event: Tutorial
When: 10:00 - 12:30
Where: 1.05

Abstract
Powering 5G applications requires end-to-end full-link energy saving design from the aspects of power supply, conversion, and power distribution. Improve the efficiency by power minimization and dynamic power management techniques have been widely explored in the past, however there is an important factor commonly ignored, which is the power conversion efficiency of a power delivery network (PDN). This article focuses on the efficiency of the PDN, introduces frequency domain techniques to optimize PDN designs and validate the efficacy of the proposed methods.

Organisers
Jose Luis Silva is currently working as Staff Applications Engineer in Monolithic Power Systems (MPS) since 2023 supporting European server and telecom group, where enhance and debug analog and digital IC products in DC/DC converters, controllers, and DrMOS applications, he also develops application reference circuits and system level power management solutions for computing power and server markets. Since 2015 Jose Luis has been working as an analog engineer focused on Power supplies and power integrity for companies such as Plexus Corporation and Intel Corporation. He has been designing power supply solutions for a broad range of product markets, including Server platforms, Network Interface Cards, Consumer electronics, and specialized test equipment.

Marlon Eguia currently works as an Applications Engineer in Monolithic Power Systems (MPS) since 2022 supporting European server and telecom group, where enhance and debug analog and digital IC products in DC/DC converters, controllers, and DrMOS applications, he also develops application reference circuits and system level power management solutions for computing power and server markets. Since 2017 Marlon has been working as a power integrity and power delivery design engineer at Intel Corporation for the data center group developing methodologies, modeling, and correlation for Intel processors and reference platforms.

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W1
Technologies and Circuits for 5G Evolution to 6G

Florinel Balteanu *(Skyworks Solutions, US)*
Andrei Grebennikov *(Sumitomo, GB)*

Event: Workshop
When: 10:00 - 12:30
Where: 1.06

Abstract
The research area of improving the performance, cost and size of 5G RF solutions and evolution to 6G is very active with many developments and it is one of the driving factors for semiconductor industry. Mobile cellular subscribers reached more than 6 billion in 2022 and 5G LTE brings high data capacity as low latency using sub-6GHz and mm-Wave spectrum. Mm-Wave up to 300GHz will play a major role in future 6G networks. The proliferation of worldwide smartphones has been in part possible due to increased computational power of CMOS technology in lower feature nodes as 3nm/7nm. This has made also possible to essentially enhance RF CMOS through digital signal processing (DSP) and digital calibration. The workshop will cover 5G semiconductor technologies and architectures currently used in RF applications and the challenges for the 5G deployment as well the evolution to 6G.

Organisers
Florinel Balteanu received the M.S. degree in electrical engineering from Polytechnic Institute, Bucharest, Romania, in 1983, and the Ph.D. degree in electrical engineering from Transylvania University, Brasov, Romania, in 1995. His work has been focused on the design of radio circuits for GPS receivers, Bluetooth transceivers and GSM/CDMA cellular transceivers. He is presently a Technical Director with Skyworks Solutions Inc., Irvine, CA and is involved in designing circuits for Envelope Tracking and Front End Modules in CMOS and SOI CMOS. He holds 88 U.S. patents, with several more pending. He is author of the chapter "Envelope Tracking Techniques" in the IET book "Radio Frequency and Microwave Power Amplifiers, Vol. 2: Efficiency and Linearity".

Andrei Grebennikov received his Dipl. Eng. degree in radio electronics from Moscow Institute of Physics and Technology, Moscow, Russia, in 1980, and Ph.D. degree in radio engineering from Moscow Technical University of Communications and Informatics, Moscow, Russia, in 1991. He obtained a long-term academic and industrial experience working with the Moscow Technical University of Communications and Informatics, Moscow, Russia, the Institute of Microelectronics, Singapore, M/A-COM, Cork, Ireland, Infineon Technologies, Munich, Germany, and Linz, Austria, Bell Labs, Alcatel-Lucent, Dublin, Ireland, and Microsemi, Aliso Viejo, California, as an Engineer, Researcher, Lecturer, and Educator. He is an author and coauthor of more than 100 papers, holds 30 European and US patents, and authored 10 books dedicated to RF and microwave circuit design. Since 2016, he has been with Sumitomo Electric Europe Ltd, Elstree, UK.

Program
https://www.esscirc-essderc2023.org/tutorials-workshops

W2
Multi-Gigabit Optical Communications for Automotive

Rubén Pérez-Aranda *(KDPOF, ES)*

Event: Workshop
When: full day, 10:00
Where: 1.07

Abstract
Automotive industry is moving towards autonomous driving, which demands a large amount of data to be processed. Optical interconnections are very well positioned because of the high required data rates for connecting sensors and electronic brains with superior EMC performance. Compared with data-centres, automotive applications require much wider range of operating temperatures (-40ºC to 125ºC) and superior reliability. A new optical physical layer standard has been developed, IEEE Std 802.3cz, supporting rates between 2.5 and 50 Gb/s. The workshop brings together points of view of the main actors involved in the complete solution, i.e. car manufacturer, network, ECU manufacturer, fibre cable interconnections, test and measurement, reliability, photonics and IC design as well as packaging.

Organiser
Rubén Pérez-Aranda is KDPOF co-founder, where he is CTO. He has served +20 years as a profile manager of R&D projects for innovative digital communication systems, covering the path from information theory based research and innovation to the integrated circuits qualification and production.

His experience covers electronics and photonics device characterization, test and modeling, communications channel modeling, error correcting codes, advance modulations, channel equalization schemes, synchronization algorithms, timing recovery algorithms, signal integrity and electro-magnetics compatibility. He is co-inventor of 9 patents.

Rubén served as comment editor and editor-in-chief of the Gigabit Ethernet over Plastic Optical Fiber standard IEEE Std 802.3bv. Recently, he was main contributor in the development of Multi-Gigabit Optical Automotive Ethernet standard IEEE Std 802.3cz.

Rubén is IEEE Senior Member and Industrial Engineer with specialty on Electronics and Automatic Control (with honors) by Universidad Politécnica de Madrid, Spain.

Program
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W3

FinFETS from Cryo-CMOS to AI

Andreas Burg *(EPFL, CH)*
Alexander Fish *(Bar Ilan University, IL)*

Event: Workshop
When: 13:30 - 18:00
Where: 5B

Abstract

Advanced silicon technology nodes are more and more based on FinFETs, which have many advantages both in density and performance as well as under cryogenic temperatures. FinFET technology has recently also become more readily available also in Europe to academia and industry opening new research and design opportunities. However, at this point, Universities still work mostly with planar technologies and have only started to engage to use FinFET. The objective of this workshop is intended to close the gap between these two realities. By showing successful recent state-of-the-art examples of FinFET designs realized in silicon we hope to spark increased awareness of the benefits of the technology in the academic community.

Organisers

Andreas Burg received his Dipl.-Ing. degree from the Swiss Federal Institute of Technology (ETH) Zurich and the Dr. sc. techn. degree from the Integrated Systems Laboratory of ETH Zurich, in 2006. He is currently a Professor at the EPFL in Lausanne, Switzerland, where he is heading the Telecommunications Circuits Laboratory. His research focuses on both algorithms and implementation aspects of Telecom systems as well as on low-power high-density digital Integrated Circuits Design. In the area of circuits for communications, his group has developed both efficient algorithms for communications, ranging from MIMO detectors to algorithms for various types of channel coding. In the area of IC design, his main contributions are in the area of approximate computing and in the design of high-density memories. His group has developed for example the highest-density embedded memories in standard CMOS processes, a technology that is currently commercialized by RAAAM Memory Technologies.

Prof. Alexander Fish received the B.Sc. degree in Electrical Engineering from the Technion, Israel Institute of Technology, Haifa, Israel, in 1999. He completed his M.Sc. in 2002 and his Ph.D. (summa cum laude) in 2006, respectively, at Ben-Gurion University in Israel. Prof. Fish's research interests include power reduction methodologies for high-speed digital and mixed signal VLSI chips, energy efficient SRAM and eDRAM memory arrays, CMOS image sensors and biomedical circuits, systems and applications and cryogenic CMOS circuits. He has authored over 190 scientific papers in journals and conferences. He also submitted more than 30 patent applications of which 22 were granted. Prof. Fish has published three book chapters and two books as an editor. Prof. Fish is a member of the Technical Committee of the European Solid-State Circuits Conference. He is also a member of the VLSI Systems and Applications and Bio-medical Systems Technical Committees of IEEE Circuits and Systems Society.

Program

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W4
Towards Self Contained Recognition Integrated Classifiers for Smart Sensors

Antoine Dupret *(CEA-Leti, FR)*
Cedric Tubert *(STMicroelectronics, FR)*

Event: Workshop
When: 13:30 - 18:00
Where: 5C

Abstract
Classifiers such as Neural Networks have become ubiquitous solutions when complex classification tasks are at stake, while hybridization and CMOS processing capabilities have paved the way towards fully integrated sensors. Not surprisingly, the convergence of the two worlds in now on but poses complex challenges: among them compactness, low power consumption and high classification ratio. This workshop aims at proving an overview of the challenges of integrated NN design, technological solutions and use cases.

Organisers
Antoine Dupret is currently working on image sensors and compact Neural Networks at the Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA), France. In 1996 he was appointed Assistant Professor with the Université de Paris 13, then Full Professor at ESIEE Engineering in 2009. He joined CEA in 2010 as senior expert in Image Sensors. He was Head of the Sensor Integration and Reliability Lab. He earned a master's and doctoral degree in electrical engineering from the Ecole Normale Supérieure de Cachan and Université de Paris Sud 11, France in 1991 and 1995, respectively.

Cedric Tubert – System & sensor architect – Analogue and Mixed Signal Group / Imaging Division – STMicroelectronics.

After earning his Ph.D. in 2010 in the field of indirect Time-of-Flight cameras based on pinned-photodiode pixels, Cedric TUBERT joined ST as a design engineer and then architect working on CMOS image sensor analogue and mixed design. Today, Cedric is a Principal Senior Member of ST's Technical Staff focusing on indirect Time-of-Flight system architecture including pixel, sensor, algorithm/ISP, RX & TX optics specifications. Cedric TUBERT received the best joint paper awards from ESSCIRC/ESSDERC 2021 in Grenoble for "Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera"

Program
https://www.esscirc-essderc2023.org/tutorials-workshops

W5
EUROPRACTICE Workshop
Design IP Sharing and Chiplets

Romano Hoofman *(IMEC, BE)*
Natalia Belova *(IMEC, BE)*

Event: Workshop
When: 10:00 - 12:30
Where: 5B

Abstract
It is hard to overestimate the value of design IP exchange as it allows research teams to share their expertise and resources to create more advanced and innovative devices. In the meantime, IP sharing through chiplets and 3D integration is getting traction with the promise to reduce costs and improve performance in various application areas. This workshop will provide a thorough overview of existing software, hardware, and cutting-edge techniques enabling chiplets and 3D integration. It will also focus on the opportunities and challenges related to the Open-Source Hardware scene and present the roadmap for establishing a European design IP exchange repository. In the European semiconductor market, IP sharing and heterogeneous integration are now strongly supported by the EUROPRACTICE service. Since 1995 EUROPRACTICE has provided over 600 academic institutions and 300 SMEs in Europe with a full range of services to design and fabricate electronic components and systems, including design tools, fabrication technologies, and training courses. Attendees are encouraged to participate in the panel discussion at the end of the workshop, where experts in the field will share their vision about lowering the barrier to sharing design IP.

Organiser
Romano Hoofman is Strategic Development Director at IMEC. IC-link since 2016. He is currently responsible for the innovation programs of the unit and for the coordination of the EUROPRACTICE Service. He started his career in industry, where he worked as a Principal Scientist at Philips Research and later on NXP Semiconductors. He covered many different R&D topics, ranging from CMOS integration, advanced packaging, thin film batteries, photovoltaics and (bio)sensors. Romano received his PhD from the Technical University of Delft in 2000, where he investigated charge transport in semi-conducting polymers. He has authored more than 30 publications and holds more than 10 patents in various research areas.

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W6
Source-Gated Transistors The Building Block of Next-Generation Thin-Film Edge Processing Systems

Radu Sporea *(University of Surrey, GB)*

Event: Workshop
When: Half day, 13:30
Where: 1.05

Abstract
Source-gated transistors (SGTs) have a relatively long history of development but only recently have mainstream technologies allowed for their effective implementation at scale. This tutorial is addressed to those interested in efficient analog and mixed signal design with advanced thin-film transistors. It provides a development progression with a forward look toward SGT application to future edge processing of sensor data, signal conditioning, and current-mode driving. Crucially, the concept can be applied in practically any material system. As such, the tutorial will present the fundamentals of contact effect engineering and modelling, design rules for successful SGT implementation, specifics of performance optimisation in organic and oxide semiconductors, and structural evolutions for additional functionality.

Organiser
Dr Radu Sporea SMIEE MIET is Senior Lecturer in Power Electronics and Semiconductor Devices at the Advanced Technology Institute (ATI), University of Surrey and holds an EPSRC Early Career Fellowship (2021-2026).

Prior to this appointment he was Royal Academy of Engineering Academic Research Fellow (2011-2016), EPSRC PhD+ Fellow (2010-2011) and PhD researcher (2006 – 2010) in the same centre. Before joining Surrey, Radu has studied Computer Systems Engineering at "Politehnica" University, Bucharest, Romania, and has worked as a Design Engineer for Catalyst Semiconductor Romania, now part of ON Semiconductor, on ultra-low-power CMOS analog circuits. Radu's was named an EPSRC Rising Star in 2014 and was the recipient of the I K Brunel Award for Engineering in 2015. He was presented the Vice Chancellor's award for Early Career Teaching in 2017 and won the Tony Jeans Inspirational Teaching distinction in 2018. In 2021, he was a finalist of the Innovator of the Year prize at Surrey. Radu chaired the 17th International Thin Film Transistor Conference (ITC2022) held as a hybrid event on the University of Surrey campus.

Current research in Radu's team focuses on three main topics:

1. Advanced large-area semiconductor device design, including transistors with increased tolerance to fabrication variability, improved energy efficiency and high gain.
2. Large area sensors and sensor arrays for smart environments, focusing on multi-modal low-cost integration in commercial manufacturing platforms and mass-market products.
3. Paper-based electronics and physical-digital interaction.

Program
https://www.esscirc-essderc2023.org/tutorials-workshops

W7
MOS-AK Workshop

Wladek Grabinski *(MOS-AK, EU)*

Event: Workshop
When: 16:00 - 18:00
Where: Auditorium III

Abstract
MOS-AK Meetings are organized with aims to strengthen a network and discussion forum among experts in the field, enhance open platform for information exchange related to compact/Spice modeling and Verilog-A standardization, bring people in the compact modeling field together, as well as obtain feedback from technology developers, circuit designers, and CAD tool vendors. The topics cover all important aspects of compact model development, implementation, deployment and standardization within the main theme - frontiers of the compact modeling for nm-scale MEMS/NEMS designs, CMOS/SOI and HEMT IC simulation. The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe, GaN, InP) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC/Bio/Med) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models, in particular using free open source PDKs.

Organiser
Wladek Grabinski received the Ph.D. degree from the Institute of Electron Technology, Warsaw, Poland, in 1991. From 1991 to 1998 he was a Research Assistant at the Integrated Systems Lab, ETHZ, Switzerland, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPFL, and was engaged in the compact MOSFET model developments supporting numerical device simulation and parameter extraction. Later, he was a technical staff engineer at Motorola, and subsequently at FSL, GMC (CH). He is now a consultant responsible for SPICE modeling, characterization and parameter extraction of MOST devices for the analog/RF IC applications using FOSS CAD/EDA tool. He is an editor of the reference modeling book Transistor Level Modeling for Analog/RF IC Design, and also authored or coauthored more than 70 papers. Wladek has established ESSDERC Track3: "Compact Modeling and Process/Device Simulation" as well as has served as a member of organization committee and TPC of ESSDERC/ESSDERC, SBMicro, LADEC, SISPAD, MIXDES Conferences. He is an IEEE EDS R8 Vice Chair also supports the EPFL IEEE Student Branch. Wladek is involved in activities of the MOS-AK Association and serves as a coordinating manager since 1999.

Program
https://www.mos-ak.org/lisbon_2023/

D1
Emulating, Listening and Communicating with Neurons

Luca Selmi *(Università degli Studi di Modena, IT)*

Event: Dissemination Workshop
When: 10:00 - 18:00
Where: 1.08

Abstract
This workshop arising from truly interdisciplinary EU projects BeFerroSynaptic, IN-FET and Crossbrain, addresses three different viewpoints showcasing the latest developments in neuromorphic systems and brain-interfacing technology. Firstly, an introductory insight will be given into aspects such as relevant signals and their timescales in biology versus artificial systems, signal encoding and interpretation. Then, presenters will showcase a selection of new nano(electronic) technology solutions under study to emulate, sense and communicate with neurons. Talks will span from material/devices to circuits, systems and integration challenges. Among these: the synaptic operation of advanced CMOS- compatible ferroelectric devices, the design and measured performance of the texel neuromorphic chip. The latest developments in high performance micro-electrode arrays and their integration with CMOS readouts will exemplify the state-of-the-art in "listening" technology. We will also highlight the challenges of "communicating" with neurons via iontronic based neuromodulation techniques, and via perspective microbot nanotechnology for detection and prevention of dysfunctional neural behaviors. Last but not the least, the need of new models and simulators in support of engineering devices for neurosciences will be addressed and exemplified.

Organiser
Luca Selmi (PhD 1992) is Professor of Electronics since year 2000In 1989-1990 he was a visiting scientist at Hewlett Packard Microwave Technology Division, USA. He served as associate editor of IEEE Electron Device Letters and in 2015 he was elevated to the IEEE Fellow grade. He served as General chair of INFOS, IEEE ICMTS and EUROSOI-ULIS conferences; as IEDM TPC member, TPC member and publications chair of the IEEE VLSI Symposium. as technical committee member of IEEE IRPS. From 2017 to 2023 he has been Director of the Italian Inter-University Consortium for Nano-Electronics (IU.net) which coordinates the operation of fourteen university groups in various fields of nanoelectronics. Luca Selmi held technical and coordination responsibilities of research units in more than 15 EU projects and coordinated one (III-V-MOS). As University professor, He activated numerous international collaboration agreements and double MSc and PhD degree initiatives.

Luca Selmi's research interests spanned various topics in Micro and Nano-electronics for switching, memory and sensing applications. In particular: modeling and simulation of silicon devices, high field transport and hot carrier effects in MOSFETs, BJTs and NVM cells; Monte Carlo transport simulation; quasi ballistic transport in nano MOSFETs, scaling, and reliability of CMOS devices. Recently his research interests extended to nanoelectronics (bio)sensors based on nanoelectrode arrays for high frequency impedance spectroscopy, neural signal recording, and to functionalized ISFETs.

Luca Selmi co-authored more than 420 papers on refereed international journals (mostly IEEE-TED, IEEE Sensor Journal, IEEE-EDL) and proceedings of major international conference and one book on "Nanoscale MOS transistors: Semiclassical transport and applications" by Cambridge University Press and a few book chapters.

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D2

Technologies, Devices, Circuits, and Algorithms for Neuromorphic Event-Based Vision System

Ari Paasio *(Kovilta Oy, FI)*
Jacek Flak *(VTT Technical Research Centre of Finland, FI)*

Event: Dissemination Workshop
When: 13:30 - 18:00
Where: 5A

Abstract
The concept of neuromorphic events can be broadened beyond the conventional intensity change detections. For higher-level cognitive tasks, events of varying complexity are refined from simpler ones. The workshop introduces complex-event neuromorphic algorithms co-developed with sensors and computing hardware. Higher-level cognition algorithms operate with lower temporal rates than those designed for reflexes requiring immediate response to sensory data. Data transmission bottlenecks affect where simple events are transformed into more complex ones. Beyond-CMOS devices are widening the capabilities of the system in comparison to CMOS-only solutions. The workshop presents ideas and outcomes from the MISEL EU-project on neuromorphic sensing and computing, with additional insights from acknowledged experts in the field.

Organisers
Dr. Ari Paasio got this D.Sc. (Tech) degree in microelectronics from Helsinki University of Technology in 1999. Since then, he has been working on integrated circuit design of massively parallel processors, thermal sensing readout optimization and ultra-low-power IoT processors for e.g. medical sensors. He acted as a professor of Microelectronics at University of Turku, Finland, between 2003 and 2020. Since 2021 Paasio has worked full time at Kovilta Oy, a Finnish sensor-processor design company, where Paasio is one of the founders and a partner.

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D3
Technologies Enabling Future Mobile Connectivity & Sensing

François Brunier *(SOITEC, FR)*
Jan Craninckx, Björn Debaillie *(IMEC, BE)*
Erkan Isa *(Fraunhofer EMFT, DE)*
Dominique Morche *(CEA-Leti, FR)*

Event: Dissemination Workshop
When: 13:30 - 18:00
Where: 1.06

Abstract
This workshop will demonstrate how European SOI technologies are currently enabling the development of mobile connectivity and sensing devices, and present alternative technologies and integration strategies to realize future (sub)THz mobile devices.

Organisers
François Brunier graduated as physics and electronics Engineer from Centrale-Supelec in 1997. From 1998 to 2002, he worked as device integration engineer for embedded DRAM products in STMicroelectronics Crolles. Since 2012, as a partnership program manager, he is in charge of European collaborative KDT programs, IPCEI and public relations.

Jan Craninckx obtained his Ph.D. degree in microelectronics from the KULeuven in 1997 and was with Alcatel Microelectronics as a senior RF engineer until 2002. He then joined IMEC (Leuven, Belgium), where he currently is IMEC fellow for RF, mm-wave, analog and mixed signal circuit design. Dr. Craninckx has authored and co-authored more than 200 papers, book chapters and patents, was Editor-in-Chief of the IEEE JSSC, and is an IEEE fellow.

Björn Debaillie leads IMEC's collaborative R&D program on cutting-edge IoT technologies, covering high speed communications, high resolution sensing, and neuromorphic computing. Björn Debaillie coordinates public funded projects and seeds new initiatives. He holds patents, received awards and authored books and international papers published in various journals and conference proceedings.

Dr. Erkan Isa (Male) is with Fraunhofer EMFT since April'13, founding the IC Design group at this center. He holds PhD'12 in Microelectronics from EPFL. Dr. Isa had served as Technical Program Chair and General Co-Chair for IEEE NEWCAS 2018 and NEWCAS 2019, respectively.

Dominique Morche received the Ph.D. degree in electronics from the Institute National Polytechnique de Grenoble, Grenoble, France, in 1994. He is currently with the Commissariat à l'énergie Atomique-Leti Minatec, Grenoble, where he is a Research Director. His current field of research is in the specification and design of RF architecture for UWB, mmwave, and the IoT systems.

Program
https://www.esscirc-essderc2023.org/tutorials-workshops

D4
European Strengths and Gaps in Emerging Semiconductor Technologies

Francis Balestra *(SINANO Institute, FR)*
Leo Saint-Martin *(DECISION, FR)*
Georgios Fagas *(Tyndall, IE)*
Roel Baets *(University Gent, BE)*

Event: Dissemination Workshop
When: 13:30 – 18h00
Where: 1.04

Abstract
International cooperation is key for speeding up technological innovation, and will allow to strengthen Europe's position in global value chains in this area, which is one of the objectives of the EU Chips Act. This SINANO/ICOS workshop will gather an overview of the main EU and International activities in leading countries in the field of semiconductors, with the most promising technologies for possible international collaborations. In particular, the future technologies in advanced computation and future technologies for advanced functionalities, covering smart sensors, smart energy, energy harvesting for autonomous systems and semiconductor-based photonics will be presented and discussed by renowned experts.

Organisers
Francis Balestra has been Director of several Laboratories. Within FP6, FP7, H2020 and Horizon Europe, he coordinated several European Projects (SiNANO, NANOSIL, NANOFUNCTION, NEREID, ICOS) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics. He is member of several European Scientific Councils, of the Advisory Committees of International Journals, of the IRDS International Roadmap Committee, and founded or organized many international Conferences, and has co-authored a large number of books and publications. He is currently Vice-President of Grenoble INP, in charge of European activities, and Director of the SiNANO Institute he founded 15 years ago.

Léo Saint-Martin is partner at DECISION Etudes & Conseil. Léo joined DECISION in 2016 to manage a team of economists and bring his expertise in market research and economic analysis in the fields of electronics components and systems. Léo is the project manager of the ICOS project (International Cooperation On Semiconductors) since 2023 on behalf of DECISION. Léo is also the project manager of the METIS project (Microelectronics Training, Industry and Skills) and of the European Chips Skills Academy project since 2019 on behalf of DECISION.

Program
https://www.esscirc-essderc2023.org/tutorials-workshops

Circuit Insights

Ali Sheikholeslami
(University of Toronto, CA)

Event: EdCom
When: Full day, 10:00
Where: Auditorium IV

Abstract
Circuit Insights is a full-day event dedicated 3rd- and 4th-year undergraduate and starting graduate students. The event, held together with all the Educational Events, on Monday, Sep. 11, 2023, will feature three talks on fundamentals of circuit design, four motivational talks on applications of circuits by industry, and a panel discussion at the end. The goal is to motivate and energize the next generation of circuit designers in Europe and in the world.

Organiser
Ali Sheikholeslami (S'98-M'99-SM'02) received the B.Sc. degree from Shiraz University, Shiraz, Iran, in 1990 and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Toronto, ON, Canada, in 1994 and 1999, respectively, all in electrical and computer engineering. In 1999, he joined the Department of Electrical and Computer Engineering, University of Toronto, as an Assistant Professor. He was promoted to the rank of Associate Professor in 2004 and to the rank of full professor in 2010.

His research interests are in the areas of analog and digital integrated circuits, high-speed signaling, and VLSI memory design (including FeRAM, SRAM, CAM, and MRAM). He currently supervises two active research groups in the areas of high-speed signaling and VLSI memories. He has collaborated with industry on various VLSI design research in the past few years, including work with Nortel and Mosaid, Canada, and with Fujitsu Labs of Japan and America. He spent his 2005-2006 research sabbatical year with Fujitsu Labs of Japan and Fujitsu Labs of America.

He served on the Memory Subcommittee of the IEEE International Solid-State Circuits Conference (ISSCC) from 2001 to 2004, and on the Technology Directions Subcommittee of the same conference from 2002 to 2005. Since 2007, he has served on the Wireline Subcommittee of ISSCC. He presented a tutorial on ferroelectric memory design at ISSCC 2002 and a tutorial on high-speed signaling at ISSCC 2008. He is an Associate Editor for the IEEE Transactions on Circuits and Systems -Part I. He was the program chair for the 34th IEEE International Symposium on Multiple-Valued Logic (ISMVL 2004) held in Toronto, Canada. He is senior member of the IEEE, and a registered professional engineer in the province of Ontario, Canada.

Dr. Sheikholeslami has received the Best Professor of the Year Award four times (in 2000, 2002, 2005, and 2007) by the popular vote of the undergraduate students in the Department of Electrical and Computer Engineering, University of Toronto. He received the 2005-2006 Early Career Teaching Award and the 2010 Faculty Teaching Award, both from the Faculty of Applied Science and Engineering at the University of Toronto, in "Recognition of Superb Accomplishment in Teaching".

Program
Chaired by *Elena Blokhina (UCD, IE)*

Circuit Insights
Fundamentals of Circuit Design

10:00 **Start Time**

10:00 - 10:10 **Welcome Remarks**
Elena Blokhina, *University College Dublin, Ireland*
John Long, *SSCS President*
João Goes, *ESSCIRC General Chair*

10:10 - 11:20
Circuit Intuitions
Ali Sheikholeslami *(University of Toronto, CA)*

11:20 - 12:30
[Title TBA]
Chris Mangelsdorf *(Analog Devices, US)*

12:30 - 13:30 Lunch

13:30 - 14:40
Sensors and Sensor Circuits [Title TBC]
Sara Pellegrini *(ST Microelectronics, FR)*

Circuit Insights
Industry Perspective: Why Circuit Design?

14:40 - 15:05
[Title TBA]
Gerard Mora-Puchalt *(Analog Devices, ES)*

15:05 - 15:30
Circuits for 5G/6G Wireless Communication
Stefan Andersson *(Ericsson, SE)*

15:30 - 16:00 Coffee Break

16:00 - 16:25
Circuits for Machine Learning
Mahmut Ersin Sinangil *(NVIDIA, US)*

16:25 - 16:50
Cryogenic CMOS Circuits for Quantum Computing [Title TBC]
Andrea Ruffino *(IBM, CH)*

16:50 - 17:35 **Panel Discussions**
Moderated by: Elena Blokhina *(UCD, IE)*

17:35 - 17:50 **Quiz/Feedback for Participant Certificates**

17:50 - 18:00 **Concluding Remarks**

18:00 **End Time**

Tuesday, September 12

Wednesday, September 13

Thursday, September 14

Tuesday, September 12

Plenary Keynote 1: José Epifânio da Franca

Session Code: A1L-0
Location: Audit. I
Time: 9:20 - 10:00
Chair(s): Jorge Fernandes, *IST, Universidade de Lisboa, INESC-ID*

9:20 European Semiconductor Innovation and Entrepreneurship 20 Years Past, 20 Years Ahead

José Epifânio Da Franca
Universidade de Lisboa, Portugal

Tuesday, September 12

Plenary Keynote 2: Muriel Médard

Session Code: A2L-0
Location: Audit. I
Time: 10:00 - 10:40
Chair(s): Andreia Cathelin, *STMicroelectronics*

10:00 Bringing Circuits and Communications Back Together, in a Modular Fashion

Muriel Médard
Massachusetts Institute of Technology, United States

Tuesday, September 12

Advanced Devices

Session Code: A3L-2
Location: Audit. III
Time: 11:10 - 12:50
Chair(s): Tibor Grasser, *TU Wien*
Claire Fenouillet-Beranger, *CEA*

11:10 Ultrathin Gate Dielectric Enabled by Nanofog Aluminum Oxide on Monolayer MoS_2
Jung-Soo Ko[1], Zichen Zhang[2], Sol Lee[3], Marc Jaikissoon[1], Robert K.A. Bennett[1], Kwanpyo Kim[3], Andrew C. Kummel[2], Prabhakar Bandaru[2], Eric Pop[1], Krishna C. Saraswat[1]
[1]Stanford University, United States; [2]University of California, San Diego, United States; [3]Yonsei University, Korea

11:30 Transport Characterization of CMOS-Based Devices Fabricated with Isotopically-Enriched ^{28}Si for Spin Qubit Applications
G. Elbaz[1], M. Cassé[2], V. Labracherie[2], G. Roussely[2], B. Bertrand[2], H. Niebojewski[2], M. Vinet[3], F. Balestro[1], M. Urdampilleta[1], T. Meunier[1,3], B. Cardoso Paz[1]
[1]Institut Néel, CNRS, Université Grenoble Alpes, France; [2]CEA-LETI, Université Grenoble Alpes, France; [3]Siquance, France

11:50 MOSFET Characterization with Reduced Supply Voltage at Low Temperatures for Power Efficiency Maximization
W.-C. Lin[1], H.-P. Huang[1], K.-H. Kao[1], M.-H. Chiang[1], D. Lu[1], W.-C. Hsu[1], Y.-H. Wang[1], W.C.-Y. Ma[2], H.-H. Tsai[3], Y.-J. Lee[4], H.-L. Chiang[5], J.-F. Wang[5], I. Radu[5]
[1]National Cheng Kung University, Taiwan; [2]National Sun Yat-sen University, Taiwan; [3]Taiwan Semiconductor Research Institute, Taiwan; [4]National Yang Ming Chiao Tung University, Taiwan; [5]Taiwan Semiconductor Manufacturing Company, Taiwan

12:10 First Foundry Platform Demonstration of Hybrid Tunnel FET and MOSFET Circuits Based on a Novel Laminated Well Isolation Technology
Kaifeng Wang[1], Yongqin Wu[2], Ye Ren[2], Renjie Wei[1], Zerui Chen[1], Jianfeng Hang[1], Zhixuan Wang[1], Fangxing Zhang[1], Lining Zhang[1], Chunyu Peng[3], Xiulong Wu[3], Le Ye[1], Kai Zheng[2], Jin Kang[2], Xusheng Wu[1], Weihai Bu[2], Ru Huang[1,4], Qianqian Huang[1,4]
[1]Peking University, China; [2]Semiconductor Technology Innovation Center, China; [3]Anhui University, China; [4]Beijing Advanced Innovation Center for Integrated Circuits, China

12:30 Impact of Layout and Channel Processing on CMOS Low Frequency Noise Variability
Fausto Simioni, Lorenzo Labate, Daniele Savio, Mariella Brizzi, Federica Ottogalli, Riccardo Marchetti, Silvia Brazzelli, Mattia Rossetti
STMicroelectronics, Italy

Tuesday, September 12

Analog-in-Memory Computing

Session Code: A3L-3
Location: Audit. IV
Time: 11:10 - 12:50
Chair(s): Cristiano Calligaro, *RedCat Devices*
Manuel Le Gallo, *IBM*

11:10 A 256-Kb Fully Row/Column-Parallel 22nm MRAM In-Memory-Computing Macro with Differential Readout for Robust Parallelization and Scale-Up

Peter Deaville, Bonan Zhang, Naveen Verma
Princeton University, United States

11:30 Compute SNR-Boosted 22 nm MRAM-Based In-Memory Computing Macro Using Statistical Error Compensation

Saion K. Roy[1], Han-Mo Ou[1], Mostafa G. Ahmed[2], Peter Deaville[3], Bonan Zhang[3], Naveen Verma[3], Pavan K. Hanumolu[1], Naresh R. Shanbhag[1]
[1]Princeton University, United States; [2]Ain Shams University, Egypt; [3]University of Illinois at Urbana-Champaign, United States

11:50 A FeFET In-Memory-Computing Core with Offset Cancellation for Mitigating Computational Errors

Lei Zhang[1,2], Pengcheng Xu[1], David Borggreve[1], Frank Vanselow[1], Ralf Brederlow[2]
[1]Fraunhofer Institute for Electronic Microsystems and Solid State Technologies EMFT, Germany; [2]Technische Universität München, Germany

12:10 AFE-CIM: A Current-Domain Compute-in-Memory Macro for Analog-to-Feature Extraction

Sudarshan Sharma, Wei-Chun Wang, Coleman Delude, Minah Lee, Nael Mizanur Rahman, Narasimha Vasishta Kidambi, Justin Romberg, Saibal Mukhopadhyay
Georgia Institute of Technology, United States

12:30 Compute-MLROM: Compute-in-Multi Level Read Only Memory for Energy Efficient Edge AI Inference Engines

Rishabh Sehgal, Rishab Mehra, Can Ni, Jaydeep P. Kulkarni
University of Texas at Austin, United States

Tuesday, September 12

ESSDERC Keynote 1: Barbara de Salvo

Session Code: A4L-0
Location: Audit. I
Time: 14:20 - 15:00
Chair(s): Merlyne De Souza, *University of Sheffield*

14:20 New Technologies and Innovative Architectures for the Augmented Reality, the Next Human-Machine Interfaces
Barbara de Salvo
META Reality Labs Research, United States

Tuesday, September 12

Memory 1

Session Code: A5L-2
Location: Audit. III
Time: 15:10 - 16:30
Chair(s): Jerome Dubois, *NXP*
Klaus Knobloch, *Infineon Technologies*

15:10 40nm SONOS Embedded Select in Trench Memory

Radouane Habhab[1,2,3], Vincenzo Della Marca[2], Pascal Masson[3], Nadia Miridi[1], Clement Pribat[1], Simon Jeannot[1], Thibault Kempf[1], Marc Mantelli[1], Philippe Lorenzini[3], Jean-Marc Voisin[1], Arnaud Regnier[1], Stephan Niel[1], Francesco La-Rosa[1]
[1]STMicroelectronics, France; [2]Aix-Marseille University, CNRS, IM2NP UMR 7334, France; [3]University of Côte d'Azur, France

15:30 One-Pulse-Programmable Multi-Level PCM/Selector Cross-Point Memory for 20 nm Half Pitch and Beyond

Yuya Matsuzawa, Yuki Ohnishi, Kazuhiro Katono, Yusuke Muto, Takayuki Tsukagoshi, Hiroki Tokuhira, Kei Sakamoto, Hisakazu Matsumori, Hiroyuki Ode, Shosuke Fujii, Hide Tanaka, Takeshi Fujimaki
Kioxia Corporation, Japan

15:50 ePCM Reliability Improvement through Active Material Carbon Implantation

Elisabetta Palumbo, Alessandro Motta, Elisa Petroni, Daniele Gallinari, Annalisa Gilardini, Amos Galbiati, Massimo Borghi, Roberto Annunziata, Andrea Redaelli
STMicroelectronics, Italy

16:20 Dynamics of Polarization Switching in Mixed Phase Ferroelectric-Antiferroelectric HZO Thin Films

Hannes Dahlberg, Lars-Erik Wernersson
Lund University, Sweden

Tuesday, September 12

Imagers & Vision Sensors

Session Code: A5L-3
Location: Audit. IV
Time: 15:10 - 16:30
Chair(s): Daniele Perenzoni, *Sony*
Cedric Tubert, *STMicroelectronics*

15:10 A 500 × 500 Pixel Image Sensor with Arbitrary Number of RoIs per Frame and Image Filtering for Center of Mass Estimation

Massimo Gottardi[1], Luca Parmesan[1], Pietro Tosato[1], Evgeny Demenev[1], Enrico Manuzzato[2], Leonardo Gasparini[1]
[1]Fondazione Bruno Kessler, Italy; [2]University of Trento, Italy

15:30 A 64×64 SPAD-Based 3D Image Sensor with Adaptive Pixel Sensitivity and Asynchronous Readout

R. Gomez-Merchan, J.A. Leñero-Bardallo, R. de la Rosa-Vidal, Á. Rodríguez-Vázquez
Universidad de Sevilla, Spain

15:50 A 100×100 CMOS SPAD Array with In-Pixel Correlation Techniques for Fast Quantum Ghost Imaging Applications

Massimo Gandola[1], Enrico Manuzzato[1,2], Matteo Perenzoni[1,3], Filippo Dal Farra[2], Valerio Flavio Gili[4,5], Dupish Dupish[4], Andres Vega[4], Thomas Pertsch[4,5], Frank Setzpfandt[4,5], Leonardo Gasparini[1]
[1]Fondazione Bruno Kessler, Italy; [2]University of Trento, Italy; [3]Sony Semiconductor Solutions Europe, Italy; [4]Friedrich-Schiller-Universität Jena, Germany; [5]Fraunhofer Institute for Applied Optics and Precision Engineering, Germany

16:20 A Time-Memory-Based CMOS Vision Sensor with In-Pixel Temporal Derivative Computing for Multi-Mode Image Processing

Dong-Woo Jee[1], Seong-Min Ko[2], Kishore Kasichainula[2], Injune Yeo[2,3], Yu Cao[2], Jae-Sun Seo[2]
[1]Ajou University, Korea; [2]Arizona State University, United States; [3]Chosun University, Korea

Tuesday, September 12

Devices & Circuits for Emerging Technologies

Session Code: A5L-4
Location: Room 5.A
Time: 15:10 - 16:30
Chair(s): Claudio Bruschini, *EPFL - Ecole Polytechnique Fédérale de Lausanne*
Louis Hutin, *LETI, Technology Research Institute*

15:10 Bias Spectroscopy of Negative Differential Resistance in GE Nanowire Cascode Circuits

Raphael Behrle[1], Martien I. Den Hertog[2], Alois Lugstein[1], Walter M. Weber[1], Masiar Sistani[1]
[1]Technische Universität Wien, Austria; [2]Institut Néel, CNRS, France

15:30 Magnetic Domain Wall Memory: A DTCO Study for Memory Applications

M. Gupta, S. Rao, G.S. Kar, S. Couet
IMEC, Belgium

15:50 A 690fJ/Bit ML-Attack-Resilient Strong PUF Based on Subthreshold Voltage Attenuator Ring with Closed-Loop Feedback

Haotao Lin, Haibiao Zuo, Qiaozhou Peng, Xiaojin Zhao
Shenzhen University, China

16:20 A 65nm RRAM Compute-in-Memory Macro for Genome Sequencing Alignment

Fan Zhang[1], Wangxin He[1], Injune Yeo[1], Maximilian Liehr[2], Nathaniel Cady[2], Yu Cao[1], Jae-Sun Seo[1], Deliang Fan[1]
[1]Arizona State University, United States; [2]State University of New York Polytechnic Institute, United States

Wednesday, September 13

Plenary Keynote 3: Eric Yang

Session Code: B1L-0
Location: Audit. I
Time: 8:30 - 9:10
Chair(s): Luis B. Oliveira, *Universidade NOVA de Lisboa*

8:30 **The Heart of Artificial Intelligence Advanced Power Semiconductors Enable Greener, Denser, and Smarter Datacenters**

Eric Yang
Monolithic Power Systems, Inc., United States

Wednesday, September 13

Compact Modeling

Session Code: B2L-2
Location: Audit. III
Time: 9:20 - 10:40
Chair(s): Benjamin Iñiguez, *Universitat Rovira*
Denis Rideau, *ST Microelectronics*

9:20 Nonlinear Compact Modeling of InP/InGaAs DHBTs with HICUM/L2

Markus Müller[1,2], Christoph Weimer[1,2], Michael Schröter[1,2]
[1]Technische Universität Dresden, Germany; [2]SemiMod GmbH, Germany

9:40 A Model for the Open-Circuit Voltage Dependence on Temperature for Integrated Diodes

Pablo Fernández-Peramo, Juan A. Leñero-Bardallo, Juan M. López-Martínez, Ángel Rodríguez-Vázquez
Universidad de Sevilla-IMSE-CNM CSIC, Spain

10:00 NITSRI-2D: A Surface Potential Based SPICE Compatible Model for pH-Sensitive FETs Based on 2-D Materials

Tamanna Nazeer, Sheikh Aamir Ahsan
National Institute of Technology Srinagar, India

10:20 Electrothermal Modeling of Junctionless Vertical Si Nanowire Transistors for 3D Logic Circuit Design

Yifan Wang[1], Chhandak Mukherjee[1], Houssem Rezgui[1], Marina Deng[1], Cristell Maneux[1], Sara Mannaa[2], Ian O'Connor[2], Jonas Müller[3], Sylvain Pelloquin[3], Guilhem Larrieu[3]
[1]University of Bordeaux, Bordeaux INP, France; [2]University of Lyon, ECL, INSA Lyon, France; [3]University of Toulouse, France

Wednesday, September 13

Biosensing & Photodetectors

Session Code: B2L-3
Location: Audit. IV
Time: 9:20 - 10:40
Chair(s): Sara Pellegrini, *STMicroelectronics*
Radu Sporea, *University of Surrey*

9:20 Hot-Carrier Degradation Modeling of DCR Drift in SPADs

Mathieu Sicre[1,2,3], David Roy[1], Francis Calmon[2]
[1]*STMicroelectronics, France;* [2]*Institut National des Sciences Appliquées de Lyon, France;* [3]*CEA-LETI, France*

9:40 On the Noise Contribution of Dielectric Interfaces in Biochemical CMOS Sensor Chips

Mathias Schulz[1], Stefan Keil[1], Simon Löhlein[1], Sourish Banerjee[2], Nicolai Simon[3], Catherine Dubourdieu[2], Volker Bucher[3], Roland Thewes[1]
[1]*Technische Universität Berlin, Germany;* [2]*Helmholtz-Zentrum Berlin für Materialien und Energie, Germany;* [3]*Hochschule Furtwangen, Germany*

10:00 Characterisation of Photodiodes in 22 nm FDSOI at 850 nm

Jelle H.T. Bakker, Mark S. Oude Alink, Jurriaan Schmitz, Bram Nauta
University of Twente, Netherlands

10:20 Ultra-High Sensitivity Silicon Nanowire Array Biosensor Based on a Constant-Current Method for Continuous Real-Time pH and Protein Monitoring in Interstitial Fluid

Y. Sprunger[1,2], L. Capua[1], T. Ernst[3], S. Barraud[3], A.M. Ionescu[1], A. Saeidi[2]
[1]*École Polytechnique Fédérale de Lausanne, Switzerland;*
[2]*Xsensio SA, Switzerland;* [3]*CEA-LETI, France*

Wednesday, September 13

Cryogenic Circuits & Systems for Quantum Computing

Session Code: B2L-4
Location: Room 5.A
Time: 9:20 - 10:40
Chair(s): Domenico Zito, *AGH University of Science and Technology*
Andrei Vladimirescu, *University of California, Berkeley*

9:20 A Cryogenic Active Router for Qubit Array Biasing from DC to 320MHz at 100 nm Gate Pitch

Baptiste Jadot[1], Marcos Zurita[1], Gérard Billiot[1], Yvain Thonnart[2], Loïck Le Guevel[1], Mathieu Darnas[3], Candice Thomas[1], Jean Charbonnier[1], Tristan Meunier[3,4], Maud Vinet[1,4], Franck Badets[1], Gaël Pillonnet[1]
[1]CEA-LETI, France; [2]CEA-LIST, France; [3]CNRS-Neel Institute, France; [4]Siquance, France

9:40 SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature

Lea Schreckenberg[1], René Otten[2], Patrick Vliex[1], Ran Xue[2], Jhih-Sian Tu[3], Inga Seidler[2], Stefan Trellenkamp[3], Lars R. Schreiber[2], Hendrik Bluhm[2], Stefan van Waasen[1,4]
[1]Forschungszentrum Jülich GmbH, Germany; [2]RWTH Aachen University, Germany; [3]University of Duisburg-Essen, Germany

10:00 A Benchmark of Cryo-CMOS 40-nm Embedded SRAM/ DRAMs for Quantum Computing

Rob A. Damsteegt, Ramon W.J. Overwater, Masoud Babaie, Fabio Sebastiano
Technische Universiteit Delft, Netherlands

10:20 A 7–10b Programmable Cryo-CMOS TI-SAR ADC for Multichannel Qubit Readout with On-Chip Background Inter-channel Mismatch Calibrations

Jaeho Lee, Kiseo Kang, Donggyu Minn, Jae-Yoon Sim
Pohang University of Science and Technology, Korea

Wednesday, September 13

Numerical & Statistical Modeling

Session Code: B3L-2
Location: Audit. III
Time: 11:10 - 12:50
Chair(s): Zlatan Stanojevic, *Global TCAD*
Viktor Sverdlov, *TU-Wien*

11:10 Understanding Distance-Dependent Variations for Analog Circuits in a FinFET Technology

Meghna Madhusudan, Jitesh Poojary, Arvind K. Sharma, Ramprasath S., Kishor Kunal, Sachin S. Sapatnekar, Ramesh Harjani
University of Minnesota, United States

11:30 Performance Comparison of SRAM Designs Implemented with Silicon-on-Insulator Nanosheet Transistors and Bulk FinFETs

Po-Chih Chen[1], Yi-Ting Wu[2], Meng-Hsueh Chiang[1]
[1]*National Cheng Kung University, Taiwan;*
[2]*Intel Corporation, United States*

11:50 A Study of the Variability and Design Considerations of Ferroelectric VNAND Memories with Polycrystalline Films Using an Experimentally Validated TCAD Model

M. Thesberg, F. Schanovsky, Z. Stanojević, O. Baumgartner, M. Karner
Global TCAD Solutions GmbH, Austria

12:10 Static and Dynamic Stochastic Analysis of a Temperature-Sensitive VO_2 Spiking Neuron

Noémie Bidoul[1], Teodor Rosca[2], Adrian M. Ionescu[2], Denis Flandre[1]
[1]*Université Catholique de Louvain, Belgium;* [2]*École Polytechnique Fédérale de Lausanne, Switzerland*

Wednesday, September 13

Digital & Analog AI Processors

Session Code: B3L-3
Location: Audit. IV
Time: 11:10 - 12:50
Chair(s): Joachim Rodrigues, *Lund University*
Gianna Paulin, *ETH Zurich*

11:10 Siracusa: A Low-Power On-Sensor RISC-V SoC for Extended Reality Visual Processing in 16nm CMOS

Moritz Scherer[1], Manuel Eggimann[1], Alfio Di Mauro[1], Arpan Suravi Prasad[1], Francesco Conti[2], Davide Rossi[2], Jorge Tomás Gómez[3], Ziyun Li[3], Syed Shakib Sarwar[3], Zhao Wang[3], Barbara De Salvo[3], Luca Benini[1,2]
[1]ETH Zürich, Switzerland; [2]University of Bologna, Italy; [3]META Reality Labs Research, United States

11:30 A 4.27TFLOPS/W FP4/FP8 Hybrid-Precision Neural Network Training Processor Using Shift-Add MAC and Reconfigurable PE Array

Sunwoo Lee[1], Jeongwoo Park[2], Dongsuk Jeon[1]
[1]Seoul National University, Korea; [2]Sungkyunkwan University, Korea

11:50 BIOS: A 40nm Bionic Sensor-Defined 0.47pJ/SOP, 268.7TSOPs/W Configurable Spiking Neuron-in-Memory Processor for Wearable Healthcare

Fengshi Tian[1,2], Xiaomeng Wang[1,2], Jinbo Chen[3], Jiakun Zheng[1,2], Hui Wu[3], Xuejiao Liu[2], Fengbin Tu[1,2], Jie Yang[3], Mohamad Sawan[3], Chi-Ying Tsui[1,2], Kwang-Ting Cheng[1,2]
[1]Hong Kong University of Science and Technology, Hong Kong; [2]AI Chip Center for Emerging Smart Systems, Hong Kong; [3]Westlake University, China

12:10 HDBinaryCore: A 28nm 2048-Bit Hyper-Dimensional Biosignal Classifier Achieving 25 NJ/Prediction for EMG Hand-Gesture Recognition

Sohum Datta, Brian Richards, Harrison Liew, Youbin Kim, Daniel Sun, Jan M. Rabaey
University of California, Berkeley, United States

12:30 An Energy-Efficient Neural Network Accelerator with Improved Protections against Fault-Attacks

Saurav Maji[1], Kyungmi Lee[1], Cheng Gongye[2], Yunsi Fei[2], Anantha P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, United States; [2]Northeastern University, United States

Wednesday, September 13

Memory Device Modeling

Session Code: B5L-2
Location: Audit. III
Time: 15:10 - 16:30
Chair(s): Sadayuki Yoshitomi, MISSING,

15:10 Complete Reconfigurable Boolean Logic Gates Based on One FeFET -One RRAM Technology

Yiqin Zeng[1], Zhetao Ding[1], Xueyang Li[1], Minglei Ma[3], Yue Peng[3], Rongzong Shen[2], Gaobo Lin[2], Chengji Jin[2], Xiao Yu[2], Bing Chen[3], Ran Cheng[1], Genquan Han[3]
[1]Zhejiang University, China; [2]Zhejiang Lab, China; [3]Xidian University, China

15:30 New Insights into Read Current Margin and Memory Window of HfO_2-Based Ferroelectric FET with Re-exploration of the Role of Ferroelectric Dynamics and Interface Charges during Readout

Chang Su, Zhongxin Liang, Zhiyuan Fu, Shaodi Xu, Kaifeng Wang, Puyang Cai, Liang Chen, Ru Huang, Qianqian Huang
Peking University, China

15:50 Comprehensive Modeling of Advanced Composite Magnetoresistive Devices

Viktor Sverdlov[1], Mario Bendra[1], Bernhard Pruckner[1], Simone Fiorentini[1], Wolfgang Goes[2], Siegfried Selberherr[1]
[1]Technische Universität Wien, Austria; [2]Silvaco Europe Ltd., United Kingdom

16:10 STT-MRAM Stochastic and Defects-Aware DTCO for Last Level Cache at Advanced Process Nodes

F. García-Redondo[1], S. Rao[2], M. Gupta[2], M. Perumkunnil[2], Y. Xiang[2], D. Abdi[2], S. Van Beek[2], S. Couet[2], M. García-Bardon[2]
[1]IMEC, United Kingdom; [2]IMEC, Belgium

Wednesday, September 13

Biosensors

Session Code: B5L-3
Location: Audit. IV
Time: 15:10 - 16:30
Chair(s): Pawel Grybos, *AGH UST*
Clara Moldovan, *EPFL*

15:10 A 256-Channel In-Pixel Electrochemical Platform in CMOS for Rapid Isothermal Genetic Amplification and Screening

Hangxing Liu, Fuze Jiang, Dongwon Lee, Yuguo Sheng, Adam Wang, Marco Saif, Ying Kong, Zhikai Huang, Thomas Burger, Jing Wang, Hua Wang
ETH Zürich, Switzerland

15:30 A 128-Channel Neural Stimulation and Recording ASIC for Scalable Cortical Visual Prosthesis

Bogdan C. Raducanu, Joan Aymerich, Wen-Yang Hsu, Patrick Hendrickx, Carolina Mora Lopez
IMEC, Belgium

15:50 A Wireless Multimodal Physiological Monitoring ASIC for Injectable Implants

Linran Zhao[1], Raymond G. Stephany[1], Yiming Han[1], Parvez Ahmmed[2], Alper Bozkurt[2], Yaoyao Jia[1]
[1]*University of Texas at Austin, United States;*
[2]*North Carolina State University, United States*

16:10 A 1.11 mm² Guidewire IVUS SoC with ±50° -Range Plane Wave Transmit Beamforming

Xitie Zhang[1], Evren F. Arkan[1], Coskun Tekes[2], Tzuhan Wang[1], F. Levent Degertekin[1], Shaolan Li[1]
[1]*Georgia Institute of Technology, United States;*
[2]*Kennesaw State University, United States*

Wednesday, September 13

RF Si Device Technology

Session Code: B5L-5
Location: Room 5.B
Time: 15:10 - 16:30
Chair(s): Nadine Collaert, *IMEC*
Cezar Zota, *IBM*

15:10 40-nm RFSOI Technology Exhibiting 90fs $R_{ON} \times C_{OFF}$ and f_T/f_{MAX} of 250 GHz/350 GHz Targeting Sub-6 GHz and mmW 5G Applications

S. Crémer[1], N. Pelloux[1], F. Gianesello[1], Y. Mourier[1], G. Haury[1], T. Chaves de Albuquerque[1], F. Monsieur[1], H. Audouin[1], C.A. Legrand[1], C. Diouf[1], J. Azevedo Goncalves[1], C. Belem Goncalves[1], C. Durand[1], N. Vulliet[1], L. Berthier[1], E. Souchier[1], P. Garcia[1], S. Jan[1], M. Hello[1], M.L. Rellier[1], P. Scheer[1], B. Duriez[2], X. Garros[2], T. Bordignon[1], F. Paillardet[1], P. Chevalier[1]
[1]*STMicroelectronics, France;* [2]*CEA-LETI, France*

15:30 22FDX® Device Optimization for mmW PA

Ming-Cheng Chang[1], Zaid Al-Husseini[1], Shafi Syed[2], Wafa Arfaoui[1], Tianbing Chen[2], Andreas Knorr[2]
[1]*GlobalFoundries, Germany;* [2]*GlobalFoundries, United States*

15:50 Improving Off-State Capacitance of SOI-CMOS RF Switches: How Good Are Air Microcavities?

Daniel Gheysens[1,2], Alain Fleury[2], Stéphane Monfray[2], Frédéric Gianesello[2], Philippe Cathelin[2], Jean-François Robillard[1], David Troadec[1], Emmanuel Dubois[1]
[1]*JUNIA, France;* [2]*STMicroelectronics, France*

16:10 Reconfigurable Ferroelectric Hafnium Oxide FeFET Fabricated in 28 nm CMOS Technology for mmWave Applications

Sukhrob Abdulazhanov[1], Quang Huy Le[1], Dang Khoa Huynh[1], Maximilian Lederer[1], Yannick Raffel[1], Kai Ni[2], Xunzhao Yin[3], Thomas Kämpfe[1], Gerald Gerlach[4]
[1]*Fraunhofer IPMS, Germany;* [2]*Rochester Institute of Technology, United States;* [3]*Zhejiang University, China;* [4]*Dresden University of Technology, Germany*

Wednesday, September 13

ESSDERC Keynote 2: Pedro Barquinha

Session Code: B6L-0
Location: Audit. I
Time: 17:00 - 17:40
Chair(s): Radu Sporea, *University of Surrey*

17:00 Oxide Thin-Film Transistors: Are We Reinventing Electronics? Or Dressing an Old Story with Today's Clothes?

Pedro Barquinha
i3N/CENIMAT, CEMOP/UNINOVA, FCT, Universidade Nova de Lisboa, Portugal

Thursday, September 14

Biomedical & Wearable Sensors

Session Code: C2L-3
Location: Audit. IV
Time: 9:40 - 10:40
Chair(s): Paul Walsh, *Infineon Technologies*
Mirjana Banjevic, *Sensirion*

9:40 A 49nV/√Hz 87.8dB-SNDR 4-Channel Digital Active Electrode System for Gel-Free and Motion-Tolerant Wearable EEG Acquisition

Chao Yuan, Yuying Li, Hao Li, Yijie Li, Zhiliang Hong, Jiawei Xu
Fudan University, China

10:00 A 3.8 mW 1.9 MΩ/√Hz Electrical Impedance Tomography Imaging with 28.4 MΩ High Input Impedance and Loading Calibration

Soyeon Um[1], Jaehyuk Lee[2], Hoi-Jun Yoo[1]
[1]*Korea Advanced Institute of Science and Technology, Korea;*
[2]*Samsung Advanced Institute of Technology, Korea*

10:20 An Electrical Impedance Spectroscopy IC with a Printable, Fractal Root Textile Sensor for Perspiration Analysis

Yung-Hua Yeh[1], Wei-Cheng Liu[1], Yi-Jie Lin[1], Yu-Siang Chou[1], Yu-Chiao Huang[1], Min-Hua Chang[1], I-Te Lin[1], Yen-Chi Chen[2], Ying-Chih Liao[2], Yu-Te Liao[1]
[1]*National Yang Ming Chiao Tung University, Taiwan;*
[2]*National Taiwan University, Taiwan*

Thursday, September 14

Memory 2

Session Code: C2L-6
Location: Room 5.C
Time: 9:40 - 10:40
Chair(s): Andrea Redaelli, *STMicroelectronics*

9:40 Integration of HfO_2-Based 3D OxRAM with GAA Stacked-Nanosheet Transistor for High-Density Embedded Memory

T. Dubreuil, S. Barraud, J.-M. Pedini, J.-M. Hartmann, F. Boulard, A. Sarrazin, A. Gharbi, J. Sturm, A. Lambert, S. Martin, N. Castellani, A. Anotta, A. Magalhaes-Lucas, A. Souhaité, F. Andrieu
CEA-LETI, France

10:00 Understanding the Impact of La Dopant Position on the Ferroelectric Properties of Hafnium Zirconate

Mihaela Ioana Popovici[1], Jasper Bizindavyi[1], Gourab De[1,2], Dae Seon Kwon[1], Gouri Sankar Kar[1], Jan Van Houdt[1,2]
[1]IMEC, Belgium; [2]KU Keuven, Belgium

Thursday, September 14

SRAM Digital Computing in Memory

Session Code: C3L-3
Location: Audit. IV
Time: 11:10 - 12:50
Chair(s): Antoine Frappé, MISSING,

11:10 FP-IMC: A 28nm All-Digital Configurable Floating-Point In-Memory Computing Macro

Jyotishman Saikia, Amitesh Sridharan, Injune Yeo, Shreyas Venkataramanaiah, Deliang Fan, Jae-Sun Seo
Arizona State University, United States

11:30 A 16nm 128Kb High-Density Fully Digital in Memory Compute Macro with Reverse SRAM Precharge Achieving 0.36TOPs/mm², 256kB/Mm² and 23.8TOPs/W

Weijie Jiang, Pouya Houshmand, Marian Verhelst, Wim Dehaene
MICAS, Katholieke Universiteit Leuven, Belgium

11:50 D6CIM: 60.4-TOPS/W, 1.46-TOPS/mm², 1005-Kb/Mm² Digital 6T-SRAM-Based Compute-in-Memory Macro Supporting 1-to-8b Fixed-Point Arithmetic in 28-nm CMOS

Jonghyun Oh, Chuan-Tung Lin, Mingoo Seok
Columbia University, United States

12:10 A 2Mbit Digital In-Memory Computing Matrix-Vector Multiplier for DNN Inference Supporting Flexible Bit Precision and Matrix Size Achieving 612 Binary TOPS/W

Mohit Gupta[1], Stefan Cosemans[1], Peter Debacker[2], Wim Dehaene[3]
[1]Axelera AI, Belgium; [2]IMEC, Belgium; [3]Katholieke Universiteit Leuven, Belgium

12:30 microASR: 32-µW Real-Time Automatic Speech Recognition Chip Featuring a Bio-Inspired Neuron Model and Digital SRAM-Based Compute-in-Memory Hardware

Dewei Wang[1], Jonghyun Oh[1], Gregory K. Chen[2], Phil Knag[2], Ram K. Krishnamurthy[2], Mingoo Seok[1]
[1]Columbia University, United States; [2]Intel Corporation, United States

Thursday, September 14

ESSDERC Keynote 3: Kenneth O

Session Code: C4L-0
Location: Audit. I
Time: 14:20 - 15:00
Chair(s): Arantxa Ori, *Universidad de Zaragoza*

14:20 Silicon Technology Innovation Opportunities for Applications at 0.1 to 1 THz beyond That for Transistors

Kenneth K. O, Muhammad Awais, Salahuddin Tariq, Matthew Stark, Suprovo Ghosh, Farooq Muhammad Musab, Behnam Pouya, Haidong Guo, Goutham Murugesan, Suhwan Lee, Sarfraz Shariff, Walter Sosa Portillo, Frank Zhang
University of Texas at Dallas, United States

Thursday, September 14

Optoelectronic Device Modeling

Session Code: C6L-1
Location: Audit. II
Time: 15:10 - 16:30
Chair(s): Wladek Grabinski, *GMC*
Fabian Bufler, *IMEC*

15:10 Near-IR Response of Highly-Strained Si Photodetector Linking First Principles and TCAD

Nicolas Roisin, Jean-Pierre Raskin, Denis Flandre
Université Catholique de Louvain, Belgium

15:30 SPICE Model of SPAD Transient Intrinsic Response Validated Using Mixed-Mode TCAD Simulations

Tom Klauner[1], Iman Sabri Alirezaei[2], Nicolas Roisin[1], Nicolas André[1], Denis Flandre[1]
[1]*Université Catholique de Louvain, Belgium;* [2]*TE Connectivity, Germany*

15:50 Extended Temperature Modeling of InGaAs/InP SPADs

E. Kizilkan[1], U. Karaca[1], V. Pešić[1], M.-J. Lee[2], C. Bruschini[1], A.J. SpringThorpe[3], A.W. Walker[3], C. Flueraru[3], O.J. Pitts[3], E. Charbon[1]
[1]*École Polytechnique Fédérale de Lausanne, Switzerland;*
[2]*Korea Institute of Science and Technology, Korea;*
[3]*National Research Council Canada, Canada*

16:10 Direct Measurements and Modeling of Avalanche Dynamics and Quenching in SPADs

D. Rideau[1], W. Uhring[3], R.A. Bianchi[1], R. Helleboid[1], G. Mugny[1], J. Grebot[1], J.R. Manouvrier[1], R. Neri[1], F. Brun[1], M. Dolatpoor Lakeh[3], S. Rink[3], J-B. Kammerer[3], C. Lallement[3], E. Lacombe[1], D. Golanski[1], B. Rae[2], T.M. Bah[1], F. Twaddle[2], V. Quenette[1], G. Marchand[1], C. Buj[4], R. Fillon[1], Y. Henrion[1], I. Nicholson[2], M. Agnew[2], M. Basset[1], R. Perrier[1], M. Al-Rawhani[2], B. Mamdy[1], S. Pellegrin[2], G. Gouget[1], P. Maciazek[2], A. Juge[1], A. Dartigues[1], H. Wehbe Alause[1]
[1]*STMicroelectronics, France;* [2]*STMicroelectronics, United Kingdom;*
[3]*ICube Laboratory, Université de Strasbourg, France;* [4]*CEA-LETI, France*

Thursday, September 14

ADC & RF Interface

Session Code: C6L-3
Location: Audit. IV
Time: 15:10 - 16:30
Chair(s): Georgi Radulov, *TU Eindhoven*
Antoine Dupret, *CEA*

15:10 An RF MEMS Sensor Driver/Readout SoC with Resonant Frequency Shift and Closed-Loop Envelope Regulation for Microplastic Detection

Seung-Beom Ku[1], Kwonhong Lee[1,2], Han-Sol Lee[1], Kyeongho Eom[1], Minju Park[1], Jinhyoung Kim[2], Cheolung Cha[2], Hyung-Min Lee[1]
[1]Korea University, Korea; [2]Korea Electronics Technology Institute, Korea

15:30 A 22dBA Digital Optical MEMS Microphone

Niccolò de Milleri[1], Andreas Wiesbauer[1], Andrea Baschirotto[2]
[1]Infineon Technologies Austria AG, Austria; [2]Università degli Studi di Milano-Bicocca, Italy

15:50 A Monolithically Integrated Electronic-Photonic Front-End Utilizing Micro-Ring Modulators for Large-Scale MM-Wave Sensing

Ruocheng Wang[1], Manuj Singh[2], Deniz Onural[2], Sidney Buchbinder[1], Hayk Gevorgyan[2], Miloš A. Popović[2], Vladimir Stojanović[1]
[1]University of California, Berkeley, United States; [2]Boston University, United States

16:10 A Linearity Improvement Method for CIS Column-Parallel SAR ADC Using Two-Step Conversion

Jaekyum Lee[1], Albert Theuwissen[1,2]
[1]Delft University of Technology, Netherlands; [2]Harvest Imaging, Belgium

Thursday, September 14

Power & RF Devices: From Substrate to Packaging

Session Code: C6L-5
Location: Room 5.B
Time: 15:10 - 16:30
Chair(s): Susanna Reggiani, *University of Bologna*
Mikael Östling, *KTH*

15:10 RF Performance of Standard, High-Resistivity and Trap-Rich Silicon Substrates Down to Cryogenic Temperature

Q. Berlingard[1,2], M. Moulin[1], J.-P. Michel[1], T. Fache[1], I. Charlet[1], C. Plantier[1], Z. Chalupa[1], J. Lugo-Alvarez[1], J.-P. Raskin[3], L. Hutin[1], M. Cassé[1]
[1]CEA-LETI, France; [2]CNRS IMEP-LAHC, France; [3]Université Catholique de Louvain, Belgium

15:30 A Composite AlGaN/cGaN Back Barrier for MM-Wave GaN-on-Si HEMTs

Rana ElKashlan[1,2], Hao Yu[1], Ahmad Khaled[1], Sachin Yadav[1], Uthayasankaran Peralagu[1], AliReza Alian[1], Nadine Collaert[1], Piet Wambacq[1,2], Bertrand Parvais[1,2]
[1]IMEC, Belgium; [2]Vrije Universiteit Brussel, Belgium

15:50 Characterization and Modeling of High Voltage MOS Robustness during Recirculation in Smart Power Technologies

Michele Basso, Marco Sambi, Andrea Marcovati
STMicroelectronics, Italy

16:10 Modeling the Temperature Dependence of TDDB in Galvanic Isolators Based on Polymeric Dielectrics

J.L. Mazzola[1], M. Greatti[1], C. Monzio Compagnoni[1], A.S. Spinelli[1], V. Marano[1], M. Lauria[1], D. Paci[2], F. Speroni[2], G. Malavena[1]
[1]Politecnico di Milano, Italy; [2]STMicroelectronics, Italy

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